d logic operations.

Date 6/4/2020

Class B.Tech 6th Sem ECE
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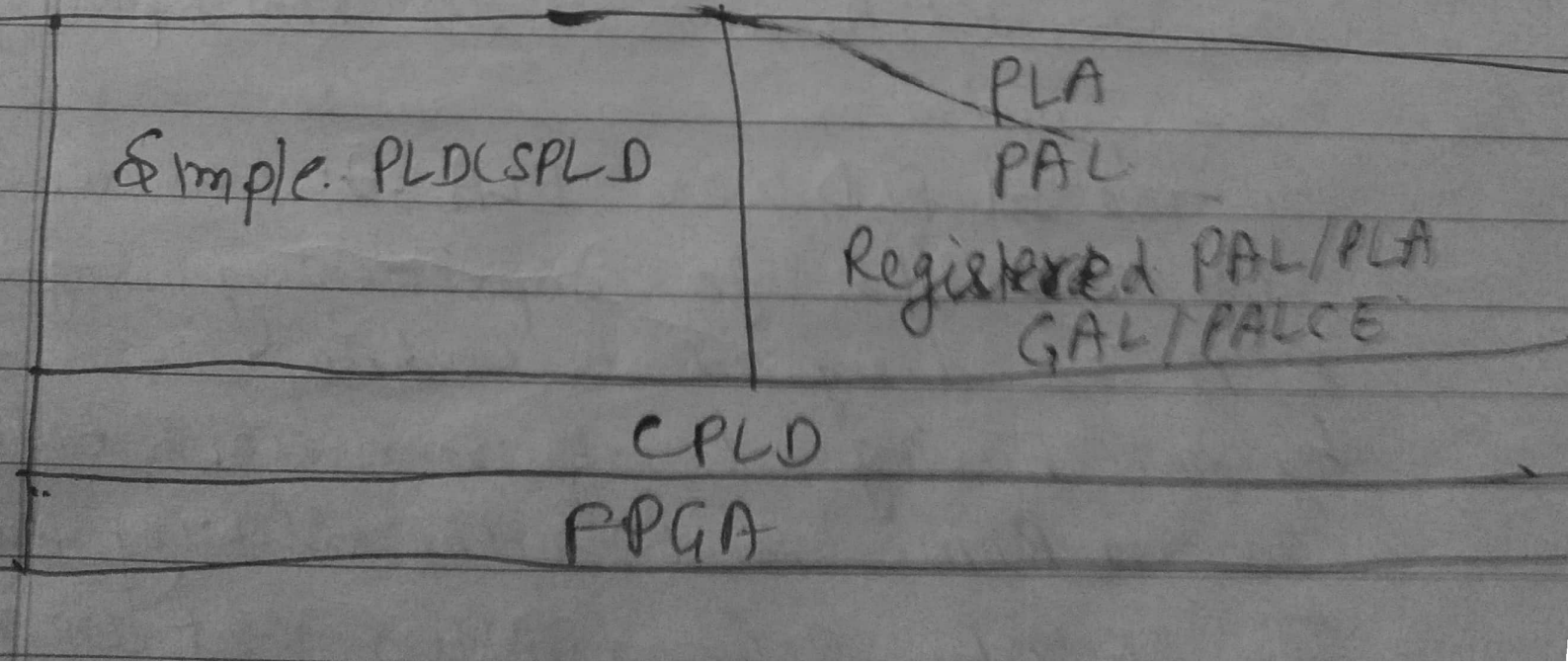
Field programmable logic array (FPLA) or simply PLA for short: A PLA consist of two levels of logic gate a programmable wired AND plane followed by programmable wire OR plane.

Drawback: (1) difficult to manufacture and introduced significant propagation delay

~~(2) and introduced significant~~

(2) they were expensive and poor speed performance to overcome these weakness Programmable Array logic

PAL (Programmable array logic) + use only logic gate (no flip flop) thus allow implementation of combinational circuit.



ROM (Read Only Memory): Memory is used for storing Binary Data. This stored data can, however can be interpreted as being the implementation of a combinational circuit.

PLA (Programmable logic array): Using ROM or EPROM to implement a combinational ckt is very wasteful because usually many location in the ROM are not used. Each storage location in a ROM represent a minterm. In practice only a small no. of these minterms are the 1-minterms for the function being implemented. As a result the ROM implementing the function

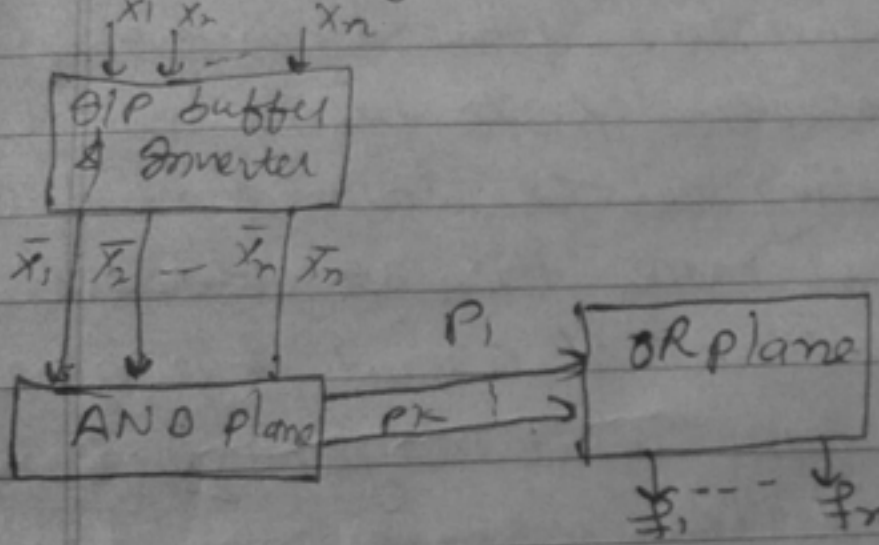
The 1st PLD were PLA. It was developed 1970 by philips for implementing logic circuit PLA are designed to reduce the wastage by not having all of minterms built in as in ROMs But rather allowing the user to specify only minterm that are needed. The PLA are described by. $n \times p \times m$

$n \rightarrow$ no. of I/P

$p \rightarrow$ no of product term

$m \rightarrow$ no. of O/P

* Main difference b/w PLA circuit and ROM circuit are for PLA circuit an AND array is used instead of Decoder
* The I/P signal are available both in the Invert and non Inverted form. The AND array allows the user to specify only the product terms needed by the function
* The OR array product portion of the circuit is similar to that of ROM allowing the user to specify which product terms to sum together



Programmable Array logic (PAL): In PLA both AND & OR array are programmable. He the programmable switches presented into two difficulties for manufacture of these devices switches wer hard to fabricate correctly switches reduced the speed performance of circuit Implemented in the PLA.

In the case of PAL the AND plane is programmable and OR plane is fixed such a chip is known as PAL device Because they are simpler to manufacture less expensive then PLA and offer better performance

CPLD (Complex Programmable logic Device)
Using Rom, PLA, PAL to implement a Comb circuit is fairly straightforward and easy to do These device can be used to implement the circuit That do not require more no. of I/P, O/P product terms that are provided in a chip These chips are limited to fairly modest size typically supporting a combinational no. of I/P plus O/P of not more then 32. However to Implement a sequential circuit or a more complex combinational circuit may require more sophisticated and larger programming device. The CPLD is Capable to Implement a ckt with upward 10,000 logic gate and logic capacity upto 50 single single SPLD.
Xilinx the world largest manufacturer of programmable semiconductor Introduced two main families XC7000 and XC9500 offering the 7200 series originally marked as the thiper EPLD and 73 Vendevelop big. plus logic

2.2.3Complex programmable logic device

A **complex programmable logic device (CPLD)** is a programmable logic device with complexity between that of PALs and FPGAs, and architectural features of both. The building block of a CPLD is the **macro cell**, which contains logic implementing disjunctive normal form expressions and more specialized logic operations.

Features in common with PALs:

- Non-volatile configuration memory. Unlike many FPGAs, an external configuration ROM isn't required, and the CPLD can function immediately on system start-up.
- For many legacy CPLD devices, routing constrains most logic blocks to have input and output signals connected to external pins, reducing opportunities for internal state storage and deeply layered logic. This is usually not a factor for larger CPLDs and newer CPLD product families.

product families.

Features in common with FPGAs:

- Large number of gates available. CPLDs typically have the equivalent of thousands to tens of thousands of logic gates, allowing implementation of moderately complicated data processing devices. PALs typically have a few hundred gate equivalents at most, while FPGAs typically range from tens of thousands to several million.
- Some provisions for logic more flexible than sum-of-product expressions, including complicated feedback paths between macro cells, and specialized logic for implementing various commonly-used functions, such as integer arithmetic.

The most noticeable difference between a large CPLD and a small FPGA is the presence of on-chip non-volatile memory in the CPLD. This distinction is rapidly becoming less relevant, as several of the latest FPGA products also offer models with embedded configuration memory.

The characteristic of non-volatility makes the CPLD the device of choice in modern digital designs to perform boot loader.