UNIT - III

CLASS - III Yr, 6th Sem

Subject - Micro controller for Embedded System

Paper Code - BT-607

Topic - System Clock and Watchdog Timer

Lecture No. - 1

Faculty Name - Dr. Nidhi Chauhan.

System clock ⇒

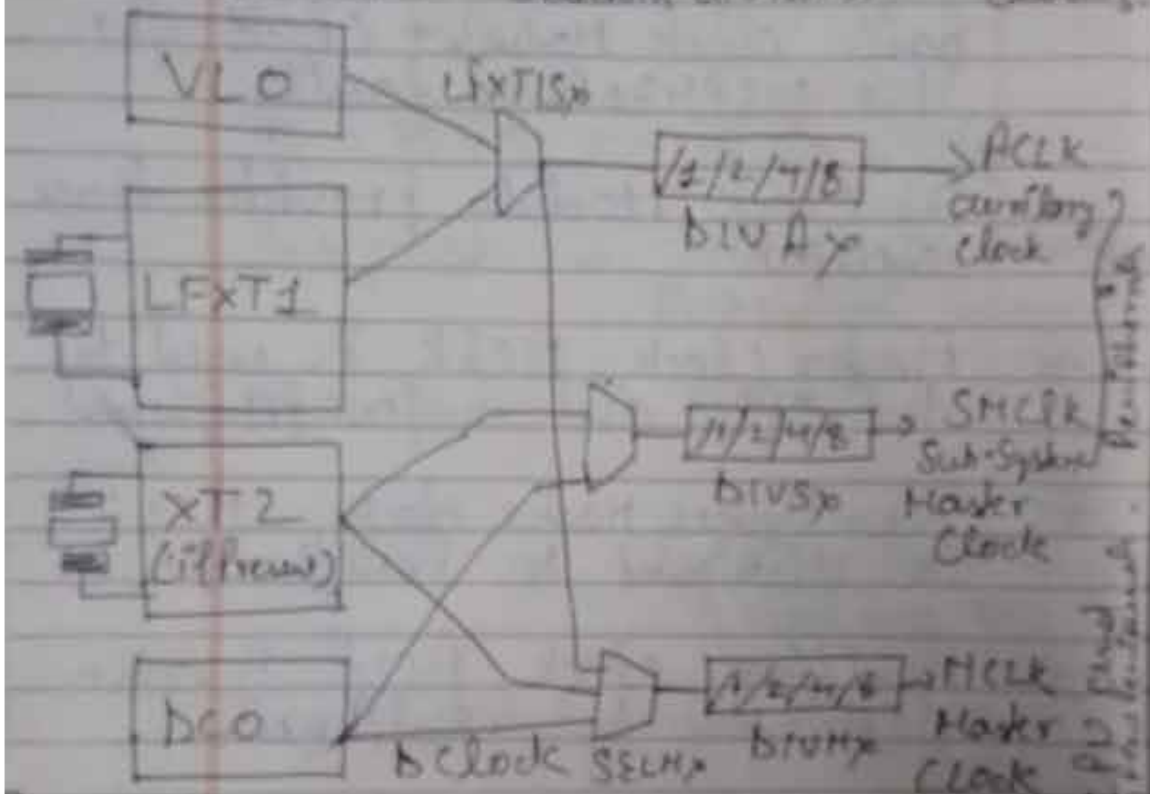
A simplified diagram of the basic clock Module + (BCM) for the MSP430F2xx family.

The clock Module provides three outputs:

* Master clock, MCLK is used by the CPU and a few peripherals.
* Sub-System Master clock, SMCLK is distributed to peripherals.
* Auxiliary clock, ACLK is also distributed to peripherals.

Most peripherals can choose either SMCLK, which is often the same as MCLK and in the Megahertz range, or ACLK, which is typically much slower and usually 32 kHz. A few peripherals such as Analog-to-digital Converters, can also use MCLK and some, such as timer have

their own clock input. The frequencies of all three clocks can be divided in the BCS+



upto four sources are available for the clock, depending on the family variant

* Low or high frequency crystal oscillator, LFXT1 — Available

The clocks BCM+ clocks.

→ ACLK auxiliary clock

→ SMCLK Sub-System Master Clock

→ MCLK Master clock

available ing on the

Crystal available

CPU and peripherals. Peripherals

in all devices, it is usually used with a low-frequency crystal (32kHz) but can also run with a high frequency crystal (typically a few MHz) in most devices. It is important to synchronize the MSP430 with other devices in system.

* High-frequency crystal oscillator, XT2- Similar to LFXT1 except that is restricted to high frequencies.

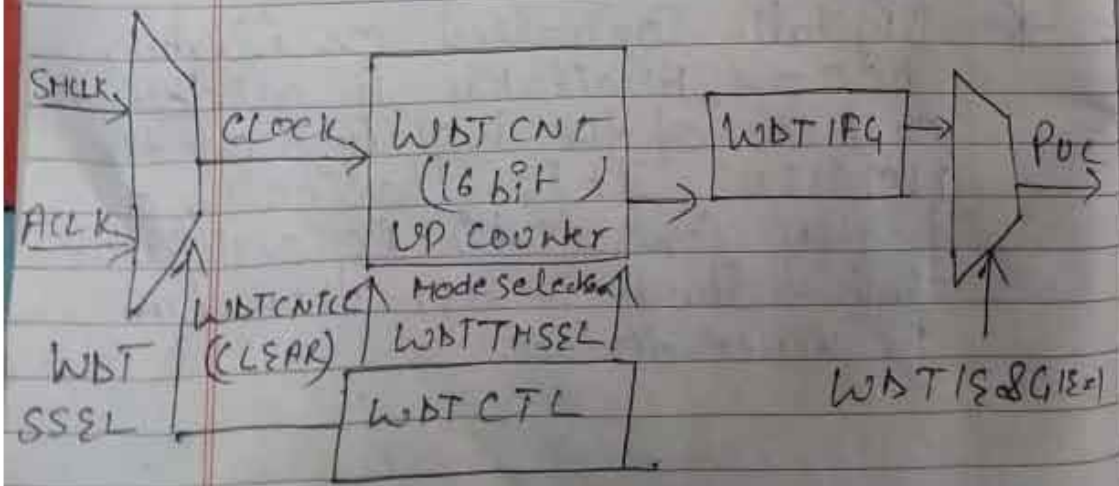
* Internal very low-power, low-frequency oscillator, VLO-

Available in only the more recent MSP430F2xx devices.

* Digitally Controlled oscillator, DCO- Available in all devices and one of the highlights of the MSP430. It is basically a highly controllable RC oscillator that starts in less than 1us in newer devices.

Topic – Watch Dog Timers

The Main Purpose of the Watchdog timer is to protect the System against failure of the Software, such as the program becoming trapped in an unintended, infinite loop. Watchdog counts up and resets the MSP430 when it reaches its limit. The code must therefore keep clearing the counter before the limit is reached to prevent a reset. The operation of the watchdog is controlled by the 16-bit register WDTCTL.



The watchdog counter is a 16-bit register WDTCNT, which is not visible to user. It is clocked from either SMCLK (default) or ACLK, according to the WDTSSEL bit. The watchdog is always active after the MSP430 has been reset. By default the clock is SMCLK, which is in turn derived from the DCO at about 1MHz. The default period of the watchdog is the maximum value of 32,768 counts, which is therefor around 32 ms. This is cleared by a power-on reset but its value is preserved during a PUC. Thus a program can check this bit to find out whether a reset arose from the watchdog.

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Lecture No – 02

Topic – Timer and Real time Clock

Faculty Name – Dr. Nidhi Chauhan

Topic

- Timer ⇒

Timer of MSP430 Series chip have two type of Timer known as Timer_A and Timer_B. Both of them are 16 Bit timers with several capture, compare channel and selectable clock sources. Time_B is slightly complex than Timer_A and offers more extensive interrupt capabilities and. Capture compare channels.

* Timer Modes -

Timer supports 4 modes of operation.

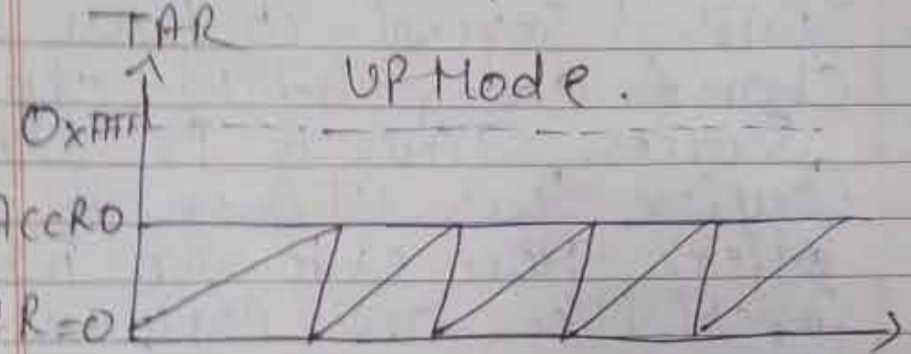
1. Stop Mode - In this mode the timer is halted.

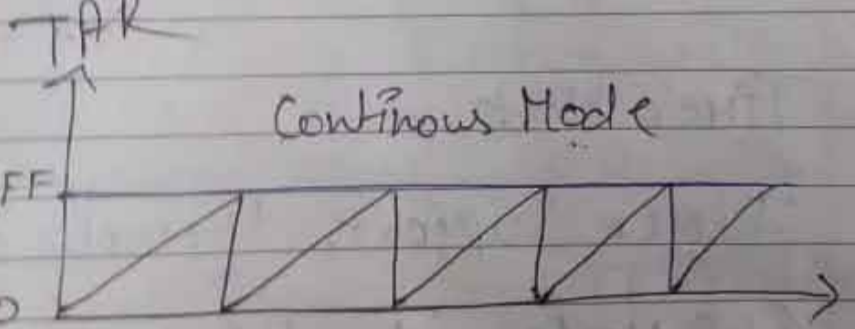
2. Up Mode - Timer repeatedly count from zero to value stored in Capture/ Compare Register of (TACCR0)

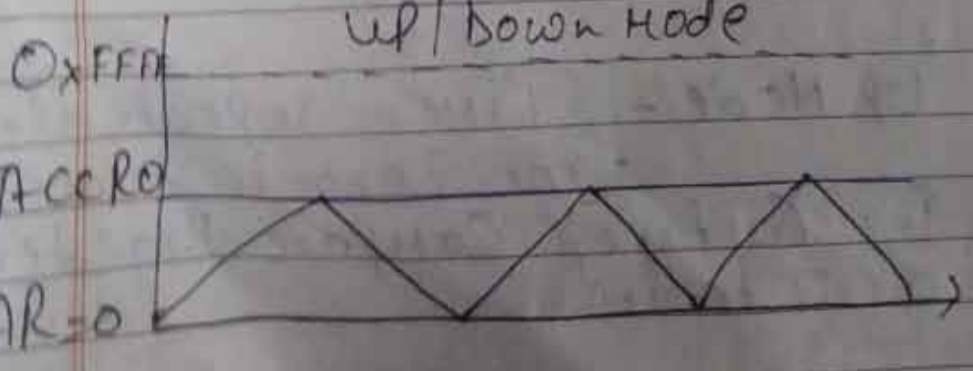
3. Continous - Timer repeatedly counts from zero to 0xFFF.

which is maximum value for 16-bit TAR.

4. Up/Down Mode - Timer repeatedly counts from zero up to the values in TACCR0 and back down to zero.





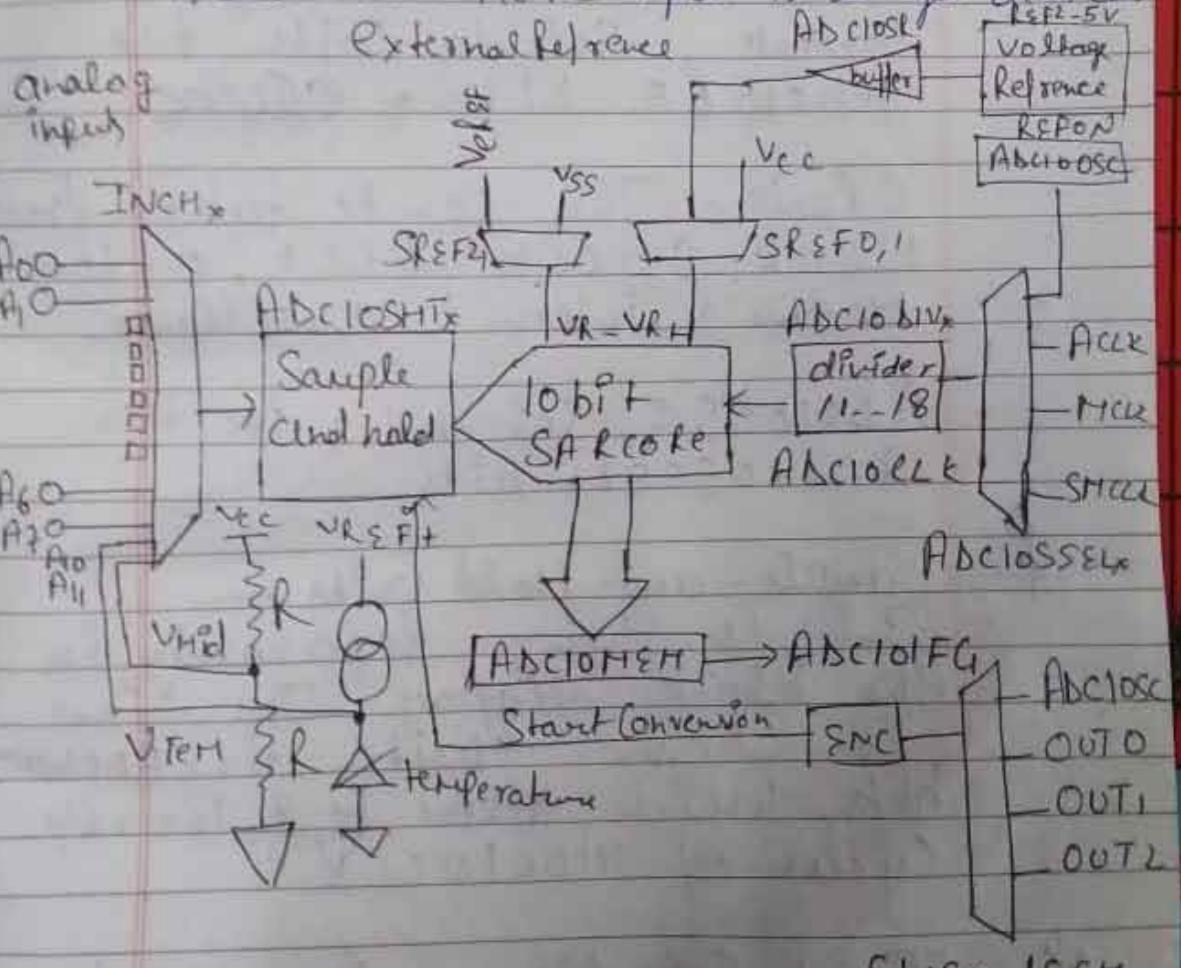


Real Time clock =>

ADC10 SAR PERIPHERAL MODULE

Simplified block diagram of the ADC10 in the F20x2.

There are More Input in larger devices External Refrence



The ADC10 Module of the MSP430F2274 supports fast 10 bit analogue-to-

digital Conversion: The Module Contains: - 10-bit SAR Core; The ADC10ON bit enables the Core and a flag ADC10BUSY is Set while Sampling and Conversion is in Progress. The result is written to ADC10 MEM in a choice of two formats, Selected with the ADC10SF bit. - Clocks

Clock - This can be taken from MCLK, SMCLK, ACLK, or the Module's internal oscillator.

ADC10DIV, Selected with the ADC10SSELx bits.

* Sample-and-Hold unit - This is Shown Separately in the block diagram. The time is Chosen with the ADC10SHTx bits, which allow 4, 8, 16 or 64 Cycles of ADC10CLK.

* Input Selection - A multiplexer Selects the input from eight external pins A0-A7 (more in larger MSP430s) and four internal Connection.

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* Conversion Trigger - A conversion can be triggered in two ways provided that the Enc bit is set. The first is by setting the ADCOSC. bit (ort Software (It clears again automatically).

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Lecture No – 03

Topic – Pulse width Modulation (PWM)

Faculty Name – Dr. Nidhi Chauhan

Topic – Pulse Width Modulation (PWM)

PWM is a scheme for varying the power provided to the load by changing the ON/OFF time of the waveform applied to the load. In this method we will be applying a square wave to the Load (here DC Motor) and by controlling the ON time (time in which wave-form is high). we will able to control the average voltage applied to the Motor and hence its speed.

As the ON time is increased the average voltage applied to the Motor also increases, hence the speed of the Motor increases. When the ON time is reduced the average voltage applied to the Motor also get reduced and the speed goes down.

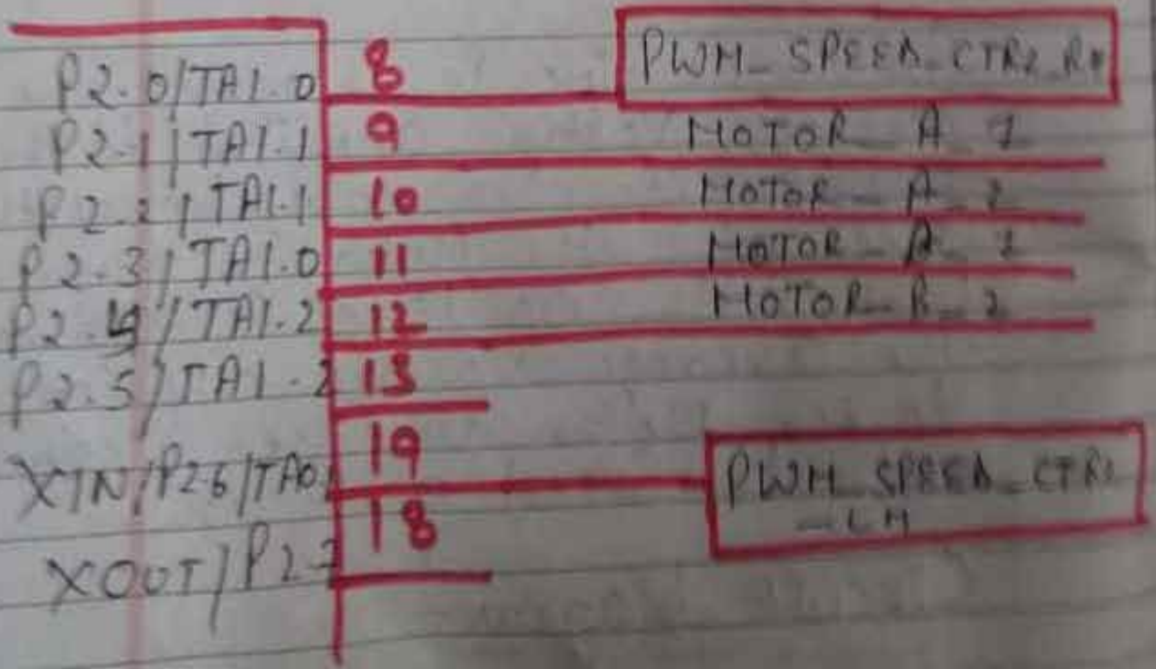
Circuit Diagram-

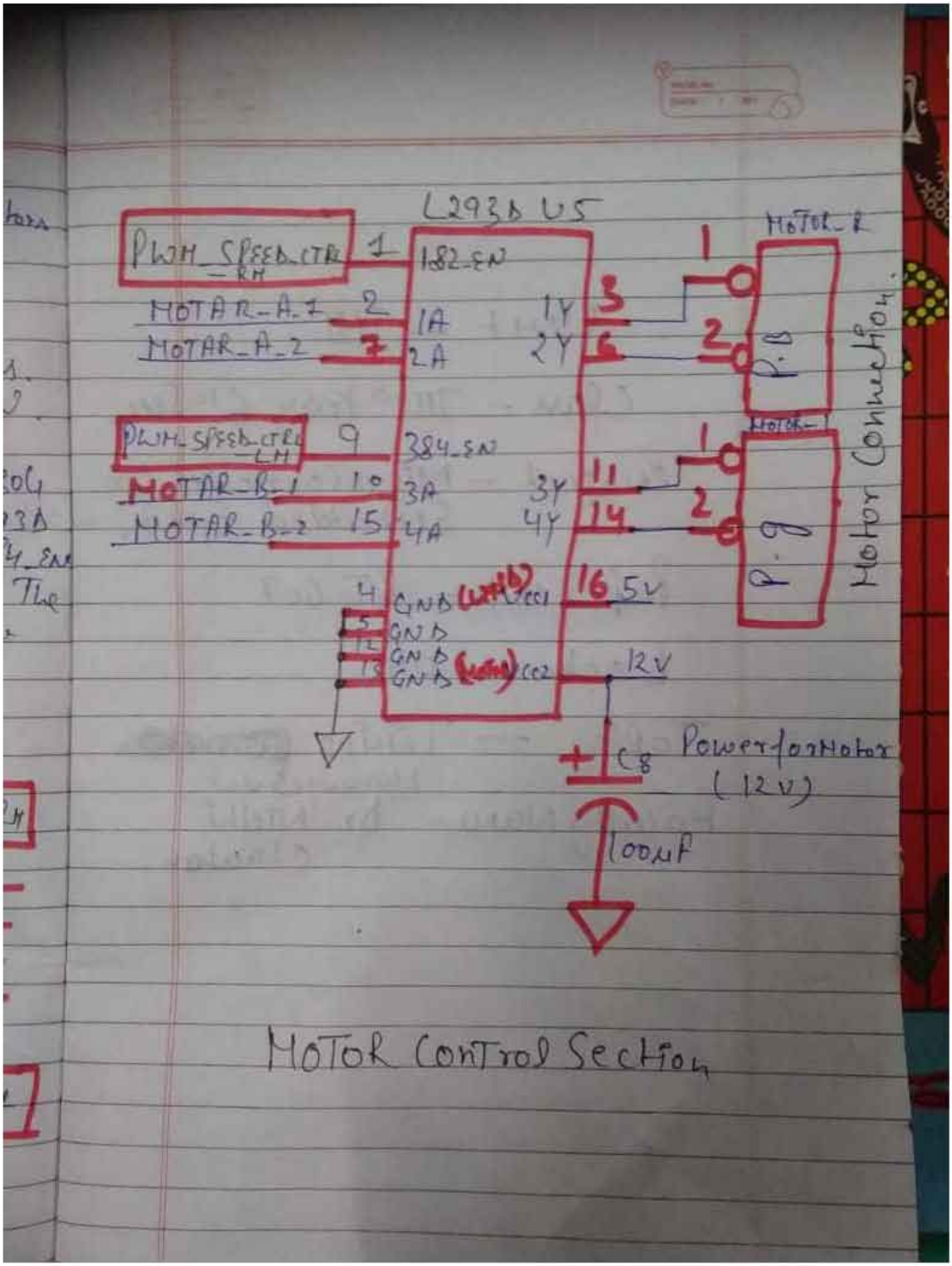
Here we will be using the L293 D Motor driver chip present

In the MSP430 Motor Control Shield to control the DC motor. To Control the speed of the Motor connected to L293D we will be applying PWM signals to the enable pins. 1&2_EN and 3&4_EN.

The Pins P2.0 and P2.6 of MSP430G2553 are Connected to L293D enable pins 1&2_EN and 3&4_EN respectively (highlighted in red). The Connection are shown in the circuit diagram.

MSP430G2553_PWM0 04





Motor Control Section