Introduction

- ASIC is an acronym for Application Specific Integrated Circuit.
- As the name indicates, ASIC is a non-standard integrated circuit that is designed for a specific use or application.
- Generally an ASIC design will be undertaken for a product that will have a large production run , and the ASIC may contain a very large part of the electronics needed on a single integrated circuit.

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- Examples for ASIC Ics are : a chip for a toy bear that talks; a chip for a satellite; a chip designed to handle the interface between memory and a microprocessor for a workstation CPU; and a chip containing a microprocessor as a cell together with other logic.

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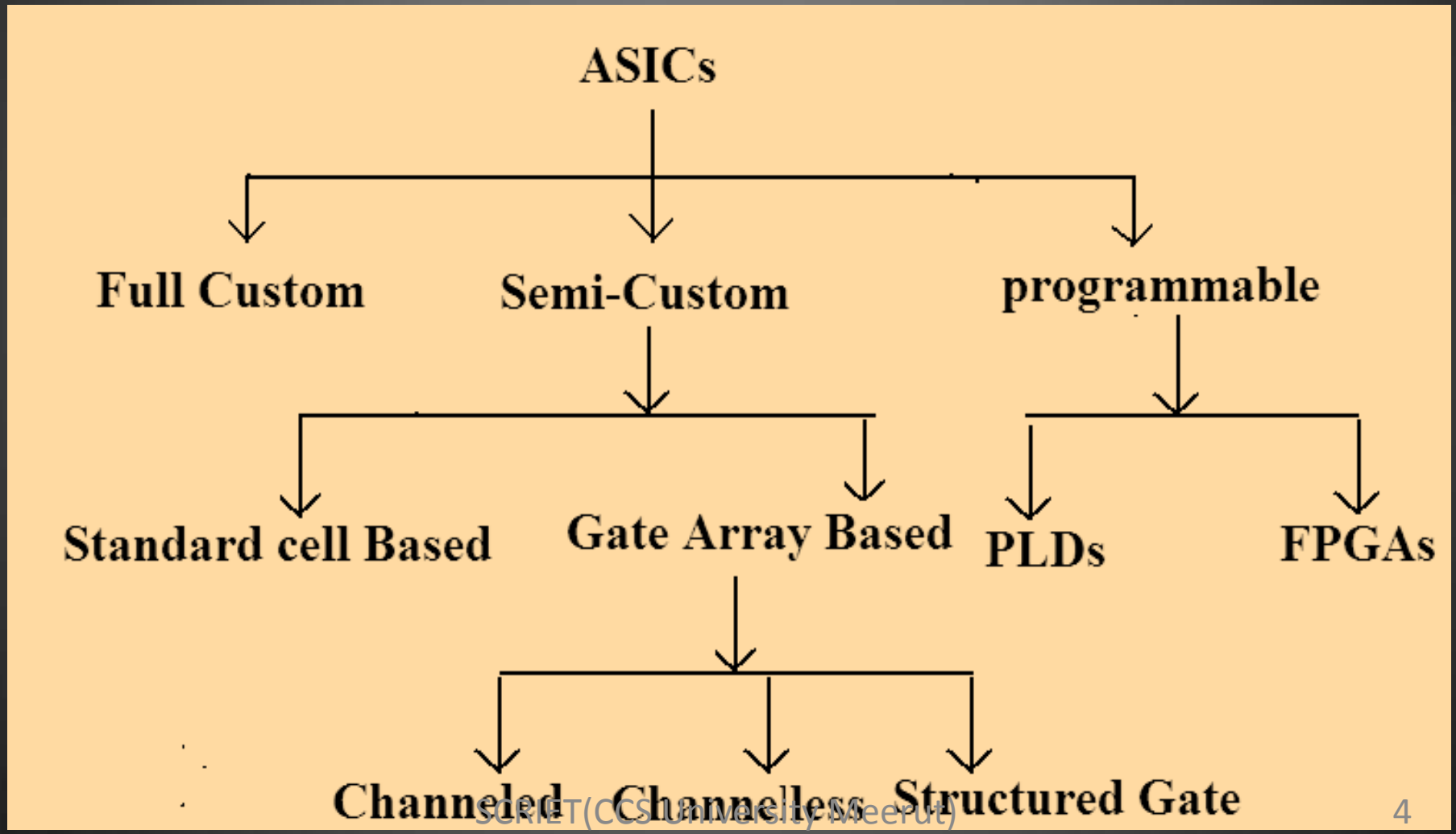
- Two ICs that might or might not be considered as ASICs are, a controller chip for a PC and a chip for a modem. Both of these examples are specific to an application (shades of an ASIC) but are sold to many different system vendors (shades of a standard part). ASICs such as these are sometimes called application-specific standard products (ASSPs).

Types of ASICs

- The classification of ASICs is shown below



Full-Custom ASICs

- A Full custom ASIC is one which includes some (possibly all) logic cells that are customized and all mask layers that are customized.
- A microprocessor is an example of a full-custom IC . Designers spend many hours squeezing the most out of every last square micron of microprocessor chip space by hand.
- Customizing all of the IC features in this way allows designers to include analog circuits, optimized memory cells, or mechanical structures on an IC, for example. Full-custom ICs are the most expensive to manufacture and to design.

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- One has to use full-custom design if the ASIC technology is new or so specialized that there are no existing cell libraries or because the ASIC is so specialized that some circuits must be custom designed.
- Fewer and fewer full-custom ICs are being designed because of the problems with these special parts of the ASIC.
- The growing member of this family, now a days is , the mixed analog/digital ASIC,

Semicustom ASICs

- ASICs , for which all of the logic cells are predesigned and some (possibly all) of the mask layers are customized are called semi custom ASICs.
- Using the predesigned cells from a cell library makes the design , much easier.
- There are two types of semicustom ASICs
- (i) Standard-cell–based ASICs
- (ii)Gate-array– based ASICs.

Standard-Cell Based ASICs

- A cell-based ASIC (cell-based or CBIC pronounced sea-bick) uses predesigned logic cells (AND gates, OR gates, multiplexers, and flip-flops, for example) known as standard cells.
- One can apply the term CBIC to any IC that uses cells, but it is generally accepted that a cell-based ASIC or CBIC means a standard-cell based ASIC.

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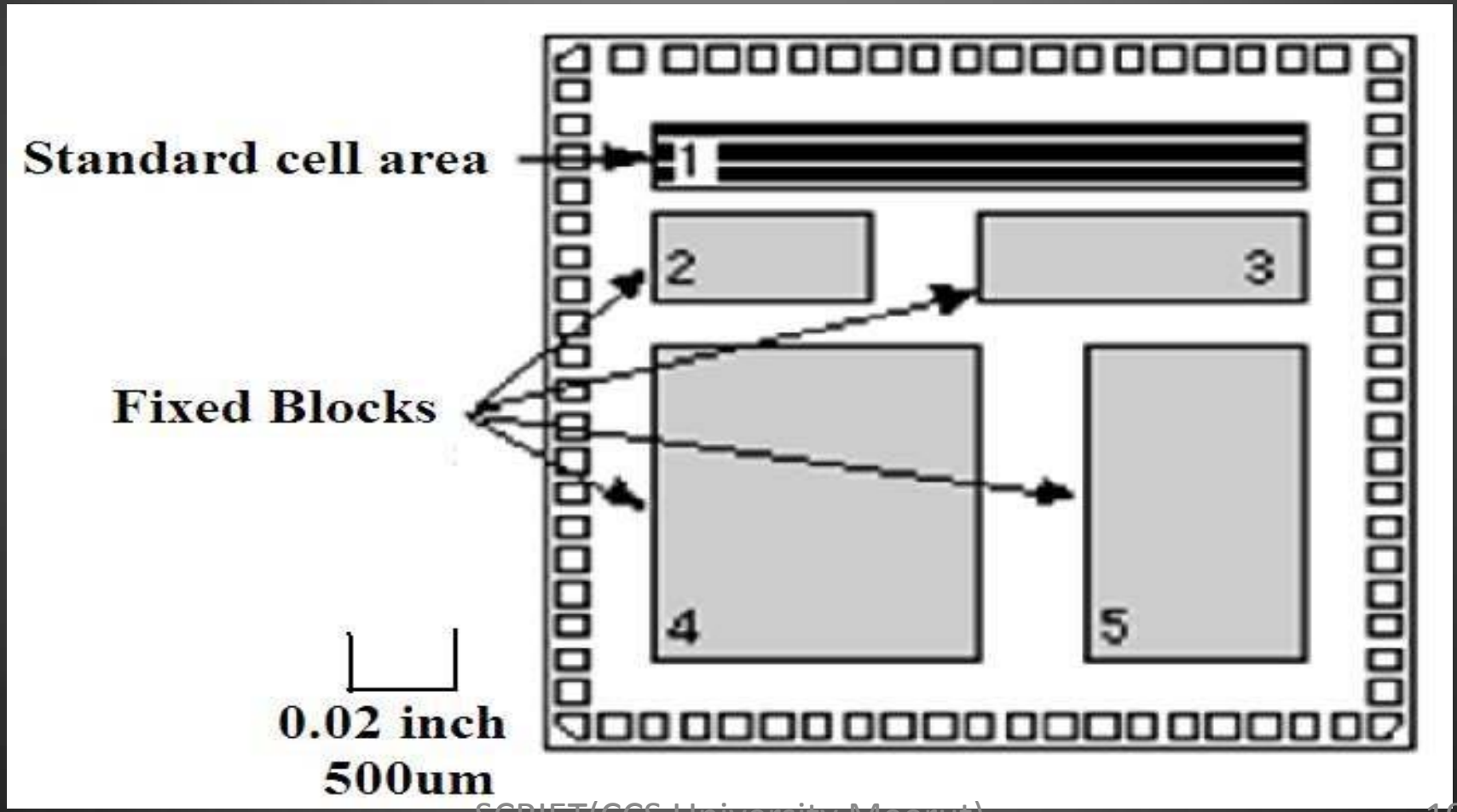
- The standard-cell areas (also called flexible blocks) in a CBIC are built of rows of standard cells like a wall built of bricks. The standard-cell areas may be used in combination with microcontrollers or even microprocessors, known as mega cells. Mega cells are also called mega functions, full-custom blocks, system-level macros (SLMs), fixed blocks, cores, or Functional Standard Blocks (FSBs).

A cell-based ASIC (CBIC) die with a single standard-cell area (a flexible block) together with four fixed blocks.



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- The disadvantages are the time or expense of designing or buying the standard-cell library and the time needed to fabricate all layers of the ASIC for each new design.

Gate-Array Based ASICs

- In a gate array (sometimes abbreviated GA) or gate-array based ASIC the transistors are predefined on the silicon wafer.
- The predefined pattern of transistors on a gate array is the base array , and the smallest element that is replicated to make the base array is the base cell (sometimes called a primitive cell).

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- The logic cells in a gate-array library are often called macros . The reason for this is that the base-cell layout is the same for each logic cell, and only the interconnect (inside cells and between cells) is customized, which is similar to a software macro.

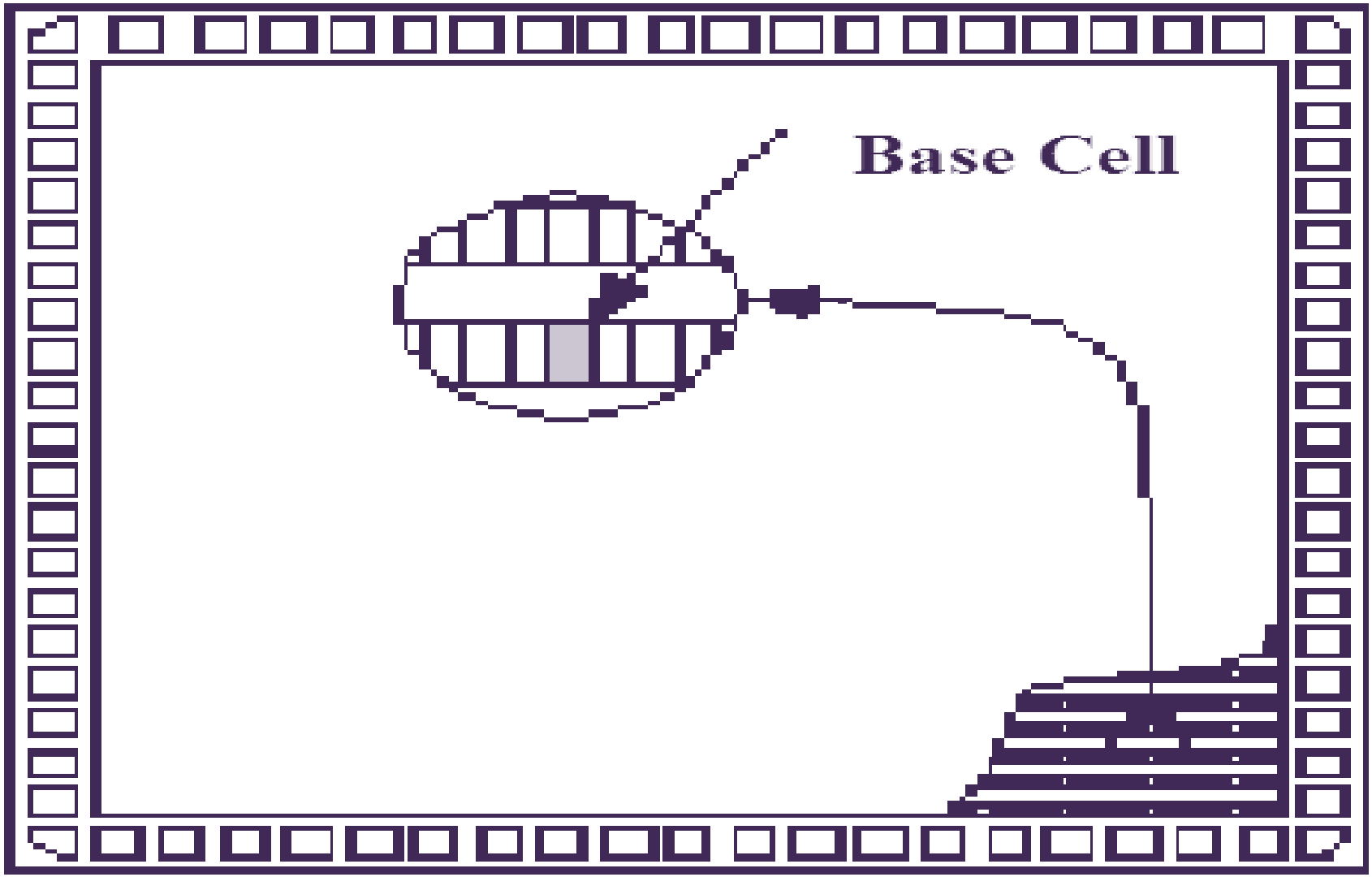
Types of MGA or Gate-array based ASICs

- There are three types of Gate Array based ASICs.
- Channeled gate arrays.
- Channelless gate arrays.
- Structured gate arrays.

Channeled gate arrays

- The channeled gate array was the first to be developed . In a channeled gate array space is left between the rows of transistors for wiring.
- A channeled gate array is similar to a CBIC. Both use the rows of cells separated by channels used for interconnect. One difference is that the space for interconnect between rows of cells are fixed in height in a channeled gate array, whereas the space between rows of cells may be adjusted in a CBIC.

A channeled gate-array



Features of MGA

- Only the interconnect is customized.
- The interconnect uses predefined spaces between rows of base cells.
- Manufacturing lead time is between two days and two weeks.

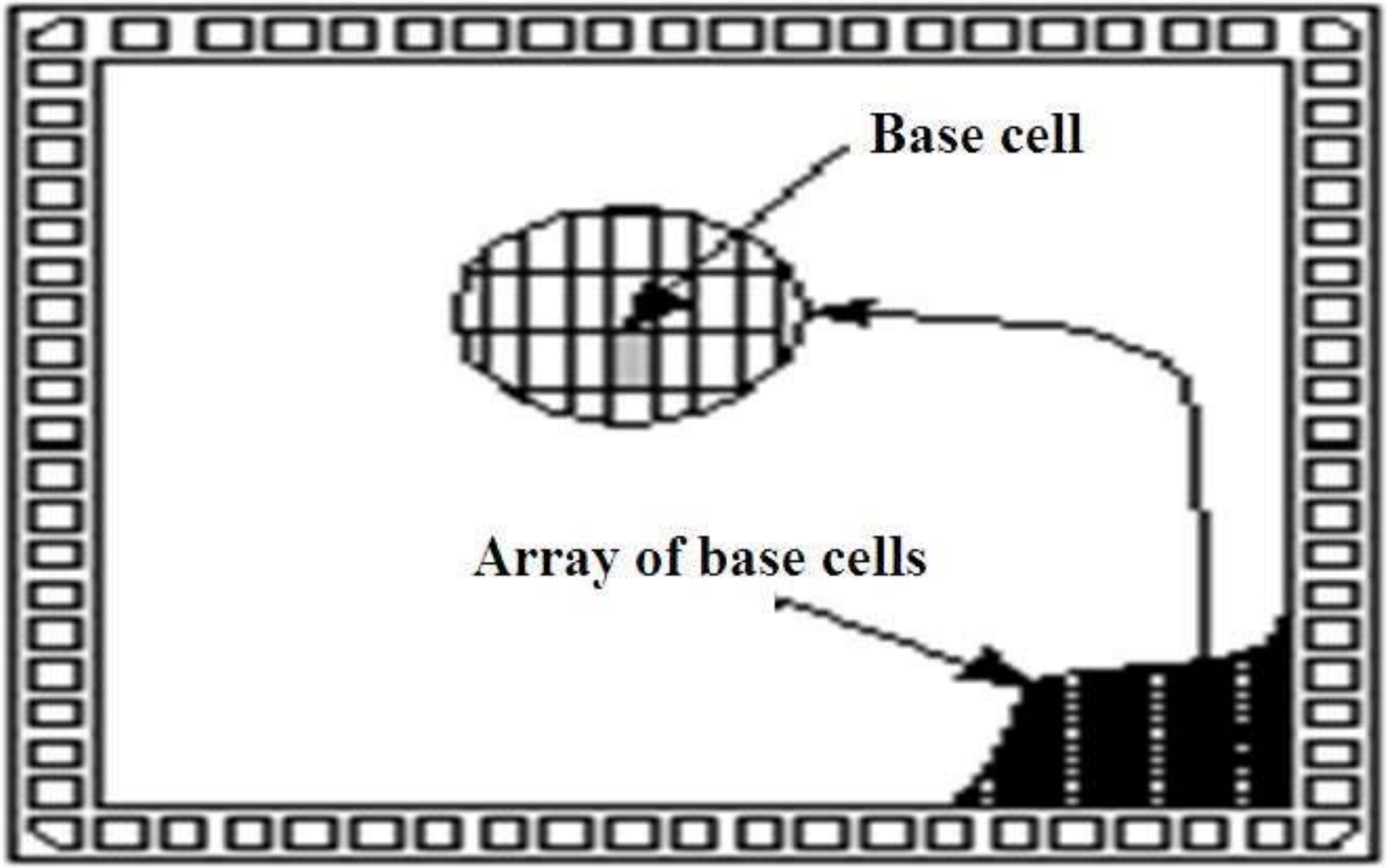
Channel less Gate Array

- This channel less gate-array architecture is now more widely used . The routing on a channelless gate array uses rows of unused transistors.
- The key difference between a channel less gate array and channeled gate array is that there are no predefined areas set aside for routing between cells on a channel less gate array. Instead we route over the top of the gate-array devices. We can do this because we customize the contact layer that defines the connections between metal 1, the first layer of metal, and the transistors.

Features of Channel less Gate Array

- Only the interconnect is customized.
- The interconnect uses predefined spaces between rows of base cells.
- Manufacturing lead time is around two days to two weeks.
- When we use an area of transistors for routing in a channel less array, we do not make any contacts to the devices lying underneath , we simply leave the transistors unused.

A channel less gate-array or sea-of-gates (SOG) array die.



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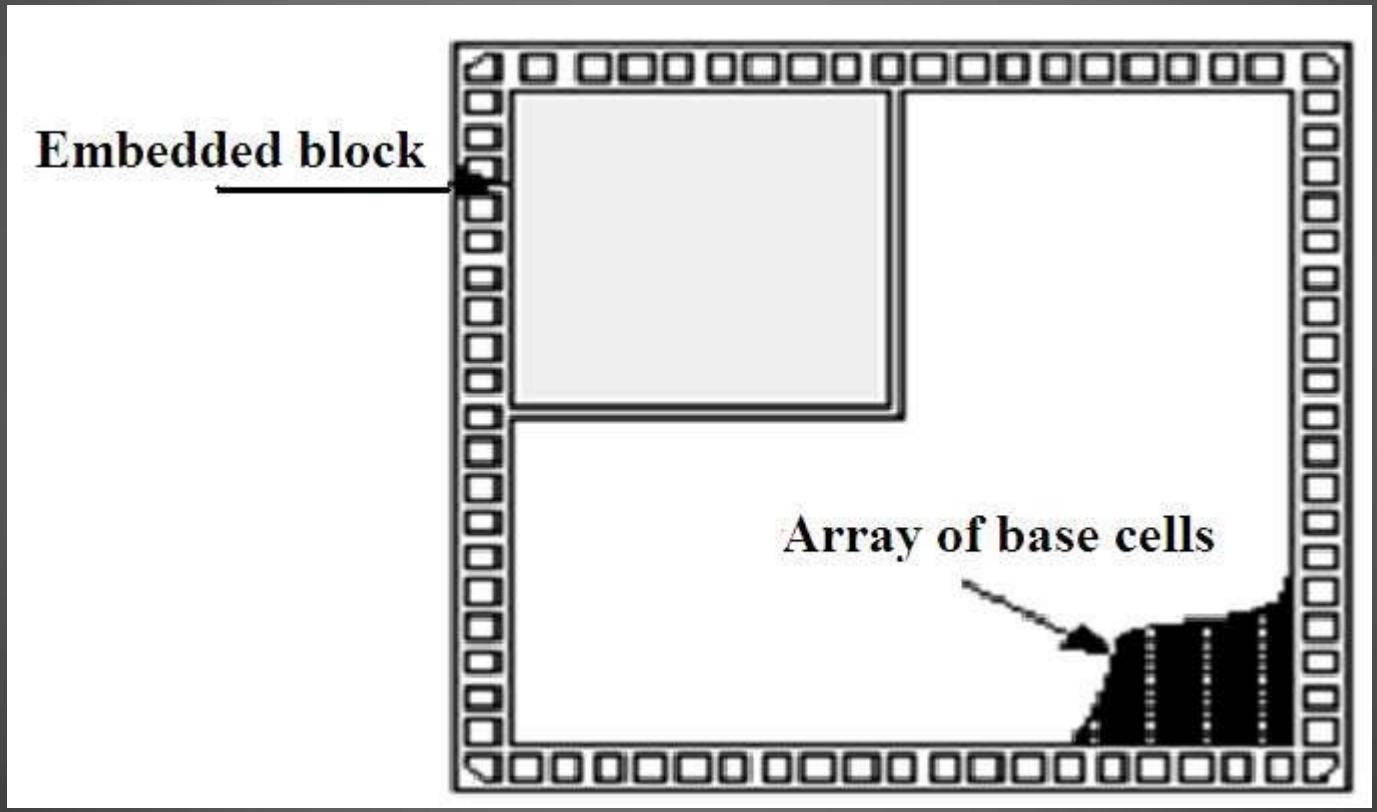
- The basic difference between a channel less gate array and channeled gate array is that there are no predefined areas set aside for routing between cells on a channel less gate array. Instead we route over the top of the gate-array devices.
- It is done like this because we customize the contact layer that defines the connections between metal1, the first layer of metal, and the transistors. When we use an area of transistors for routing in a channel less array, we do not make any contacts to the devices lying underneath; we simply leave the transistors unused.

Structured Gate Array

- This design combines some of the features of CBICs and MGAs.It is also known as an embedded gate array or structured gate array(also called as master slice or master image).
- One of the limitations of the MGA is the fixed gate-array base cell. This makes the implementation of memory, difficult and inefficient.
- In an embedded gate array some of the IC area is set aside and dedicate it to a specific function. This embedded area either can contain a different base cell that is more suitable for building memory cells, or it can contain a complete circuit block, such as a microcontroller.

A structured or embedded gate-array die showing an embedded block in the upper left corner



Features of Structured Gate Array

- Only the interconnect is customized.
- Custom blocks (the same for each design) can be embedded.
- Manufacturing lead time is between two days and two weeks.
- An embedded gate array gives the improved area efficiency and increased performance of a CBIC but with the lower cost and faster turn around of an MGA.
- The disadvantage of an embedded gate array is that the embedded function is fixed.

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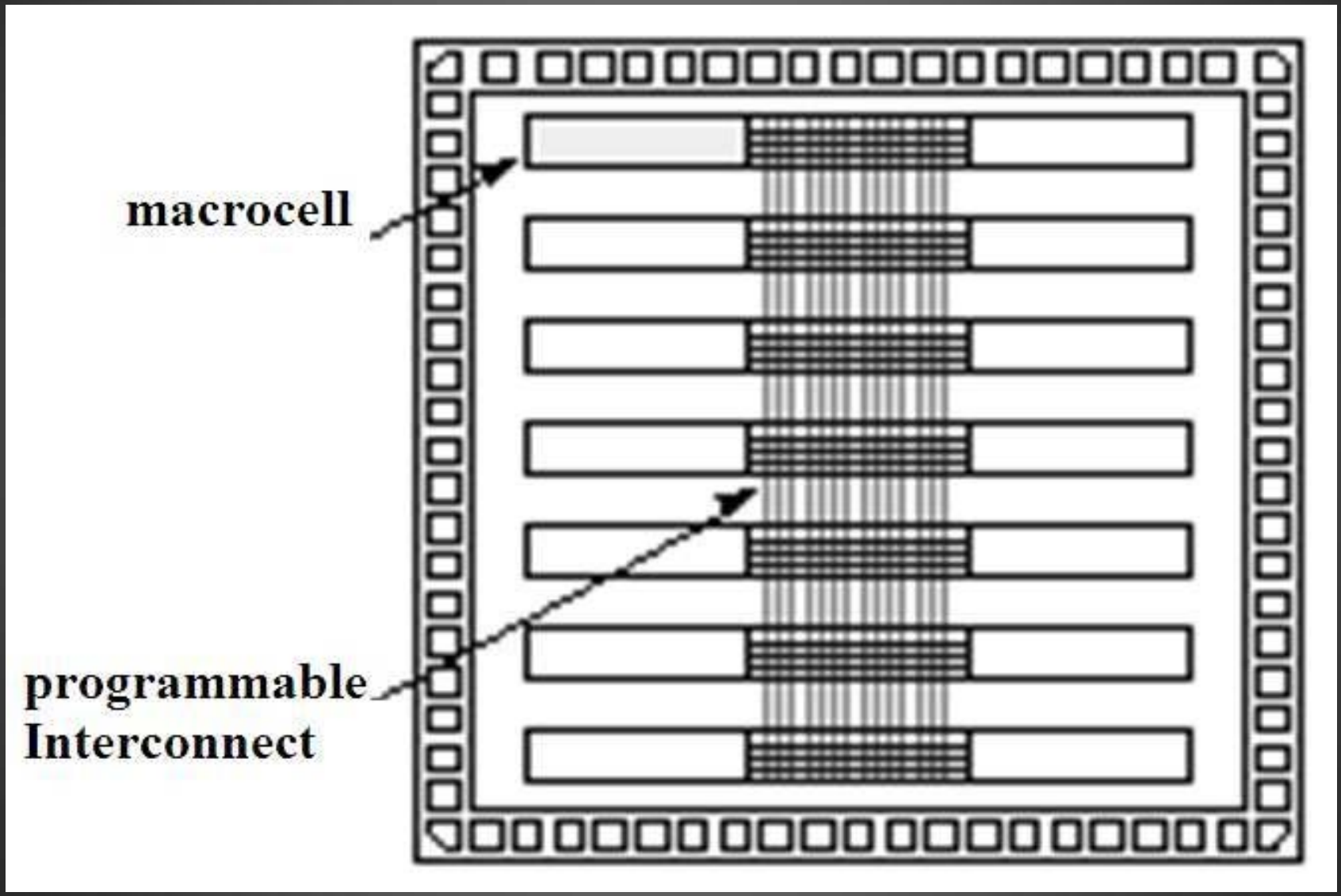
- For example, if an embedded gate array contains an area set aside for a 32 k-bit memory, but we only need a 16 k-bit memory, then we may have to waste half of the embedded memory function. However, this may still be more efficient and cheaper than implementing a 32 k-bit memory using macros on a SOG array

Programmable Logic Devices

- Programmable logic devices (PLDs) are standard ICs that are available in standard configurations.
- However, PLDs may be configured or programmed to create a part customized to a specific application, and so they also belong to the family of ASICs.
- PLDs use different technologies to allow programming of the device.

A programmable logic device (PLD) die.



Featuresof PLDs

- No customized mask layers or logic cells
- Fast design turnaround
- A single large block of programmable interconnect
- A matrix of logic macro cells that usually consist of programmable array logic followed by a flip-flop or latch

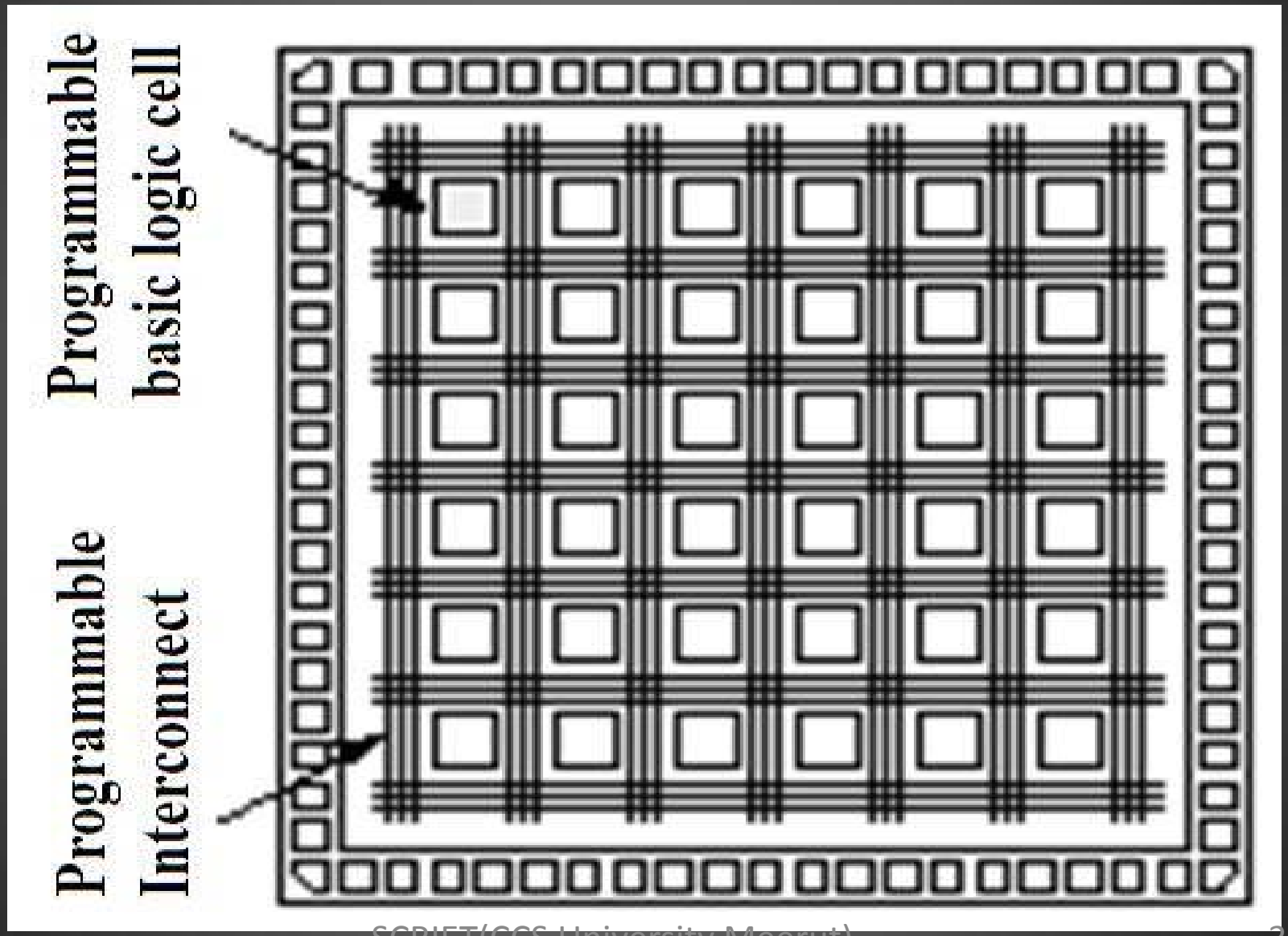
Field-Programmable Gate Arrays(FPGAs)

- FPGAs are the newest member of the ASIC family and are rapidly growing in , replacing TTL in microelectronic systems. Even though an FPGA is a type of gate array, we do not consider the term gate-array based ASICs to include FPGAs.
- There is very little difference between an FPGA and a PLD .An FPGA is usually just larger and more complex than a PLD. In fact, some vendors that manufacture programmable ASICs call their products as FPGAs and some call them as complex PLDs .

Characteristics of an FPGA

- None of the mask layers are customized.
- There is a method for programming the basic logic cells and the interconnect.
- The core is a regular array of programmable basic logic cells that can implement combinational as well as sequential logic (flip-flops).
- A matrix of programmable interconnect surrounds the basic logic cells.
- Programmable I/O cells surround the core.
- Design turnaround is a few hours.

Field-programmable gate array (FPGA) die.



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Examples of SRAM based FPGA families are

- Altera FLEX family
- Atmel AT6000 and AT40K families
- Lucent Technologies ORCA family
- Xilinx XC4000 and Virtex families

Examples of Anti-fuse based FPGA families are

- Actel SX and MX families
- Quick logic pASIC family

CPLDs vs. FPGAs

	CPLD	FPGA
• **Architecture**	PAL-like	Gate Array-like
• **Density:**	Low to medium 12 22V10s or more	Medium to high up to 1 million gates
• **Speed:**	Fast, predictable	Application dependent
• **Interconnect:**	Crossbar	Routing
• **Power Consumption:**	High	Medium

Thank You