

'Design of combinational circuit using CPLD'

Introduction:

- CPLD stands for Complex Programmable Logic Devices
- CPLD is a programmable logic Device with complexity between that of PALs and FPGAs.
- It is a combination of a fully programmable AND/OR array and a bank of macrocells.
- The AND/OR array is reprogrammable.
- Macrocells are functional blocks that perform combinatorial or sequential logic, and also have the added flexibility for true or complement, along with varied feedback paths.

Pin Diagram:

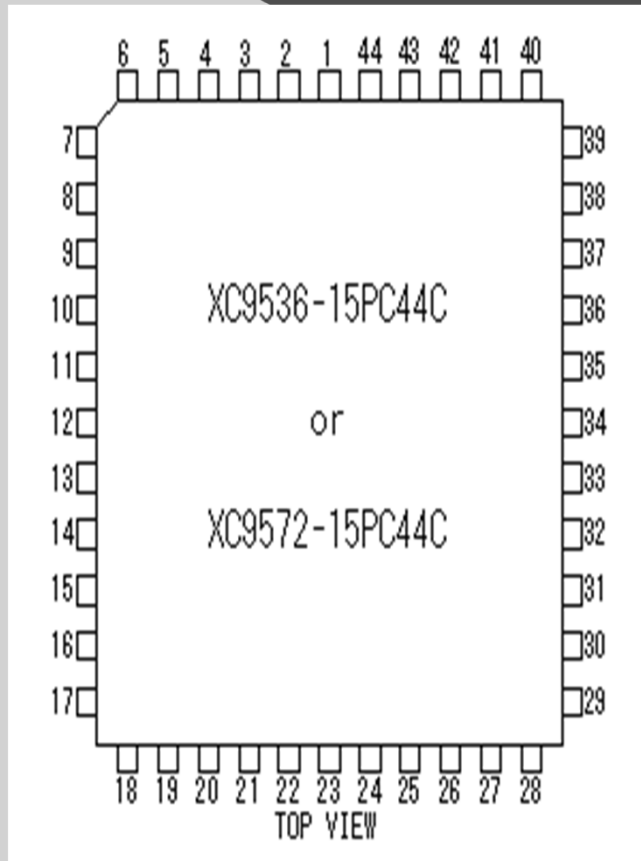


Fig. Pin Diagram of
CPLD(XC9572-15PC44C)

Pin No(21,41)= VCC(Dedicated Power Pin)

Pin No(23,31,10)= GND(Dedicated Ground Pin)

Pin No(32)= 3.3v

Pin No(1-9,11-14,18-20,22,24-29,33-40,42-44)= Data Pin(32 Input Pins)

Pin No(15)= TD1(Test Data In, JTAG Pin)

Pin No(16)= TMS(Test Mode Select, JTAG pin)

Pin No(17)= TCK(Test Clock, JTAG Pin)

Pin No(30)= TD0(Test Data Out, JTAG Pin)

Architecture:

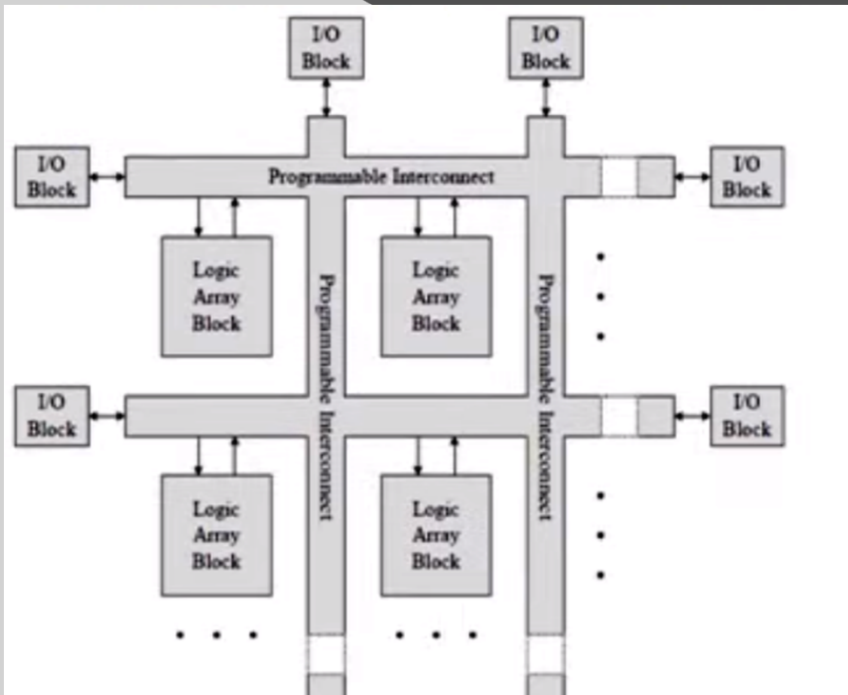


Fig. Architecture of CPLDs

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- CPLDs can be use for combinational and sequential logic circuit.
- Logic Array block(LAB) consist 16 marcocells.
- In I/O block, it is a programmable Input and output block for Input, Output and both are.
- Each LAB, memory element and I/O blocks connected with programming interconnect.

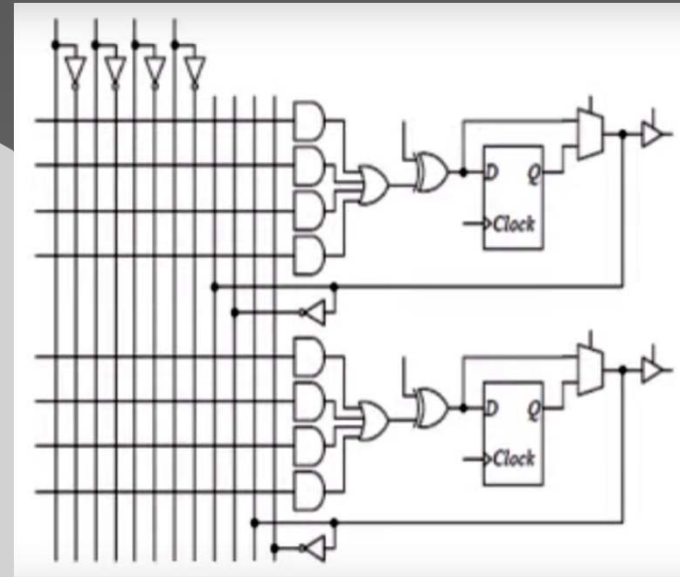


Fig. Logic Diagram of 2 marcocells

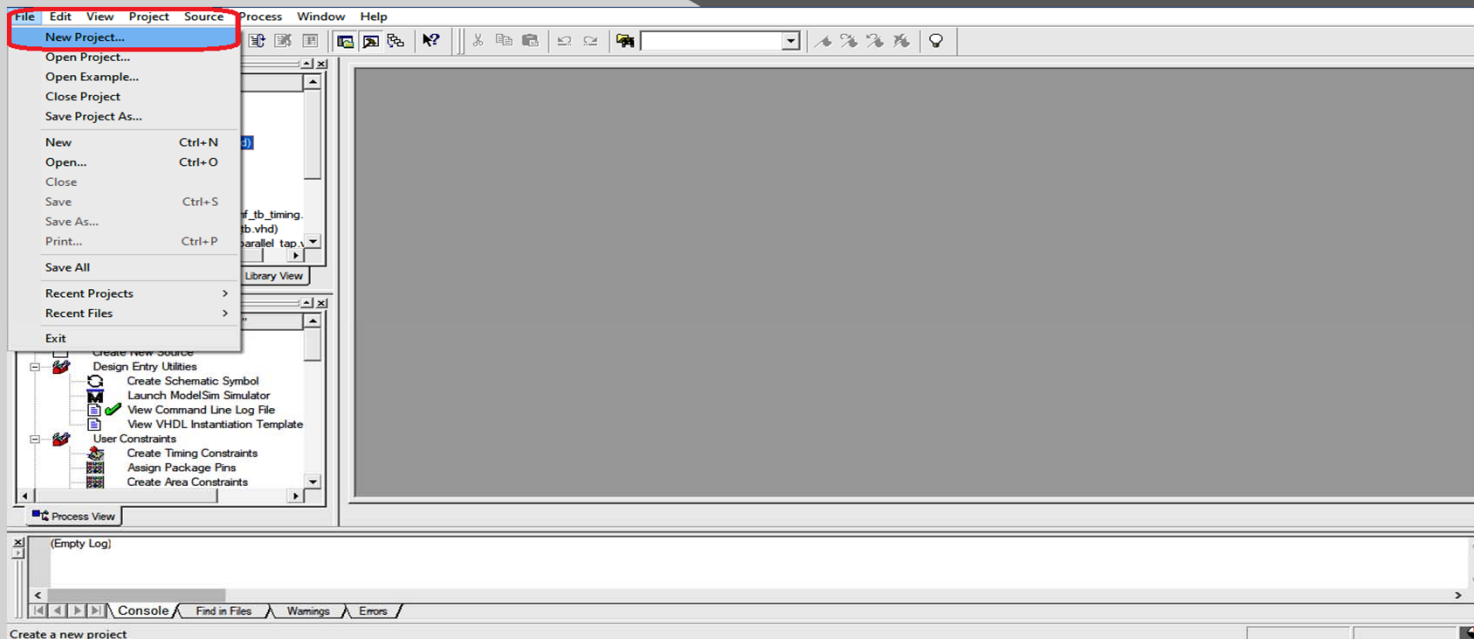
Designing of Combinational Circuit Using CPLDs:

Let's assume we are going to design And Gate using CPLDs.

Here Few Steps to design

Step1. Open Project Navigator which is appear in your Desktop Screen

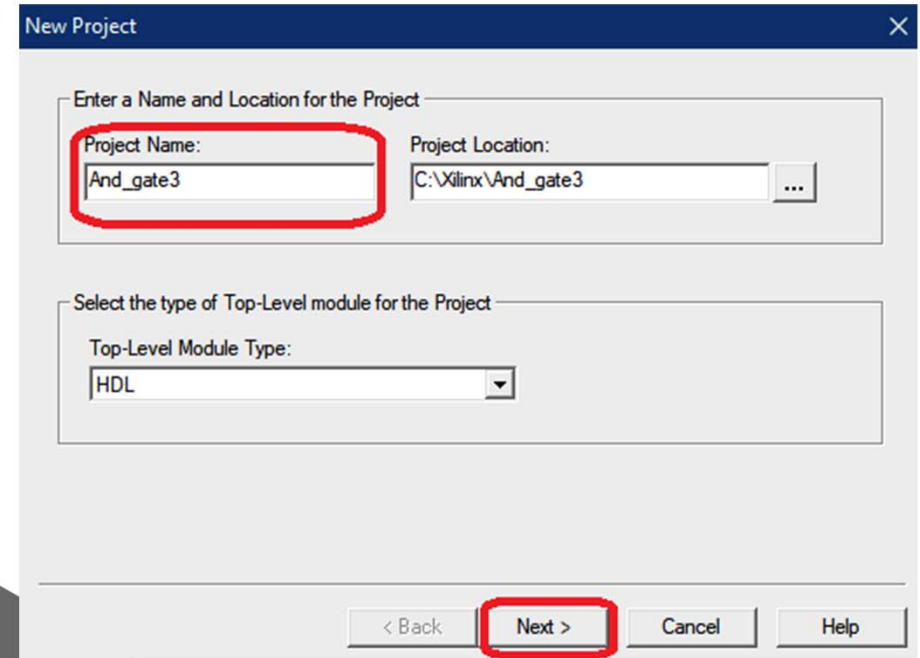
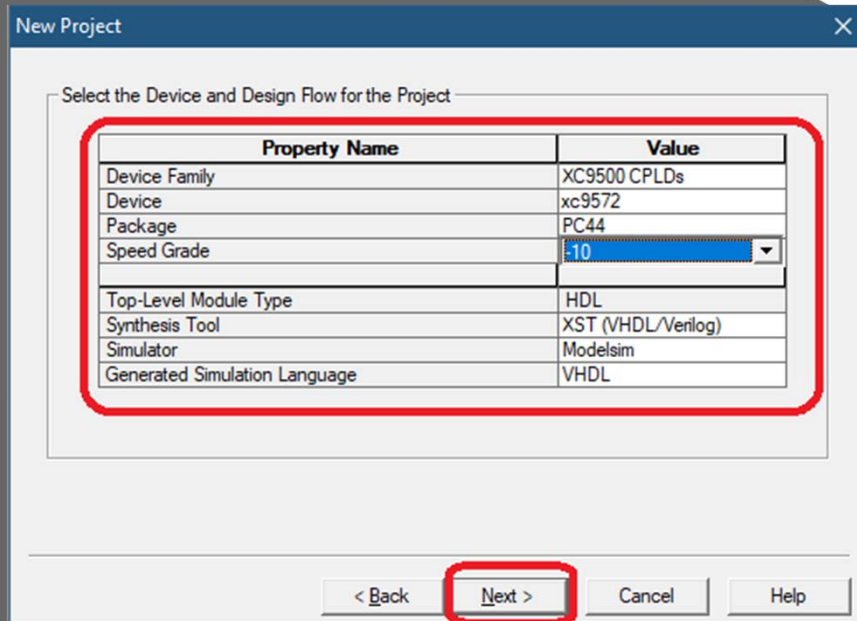
Step2. Go to File and Select New Project.



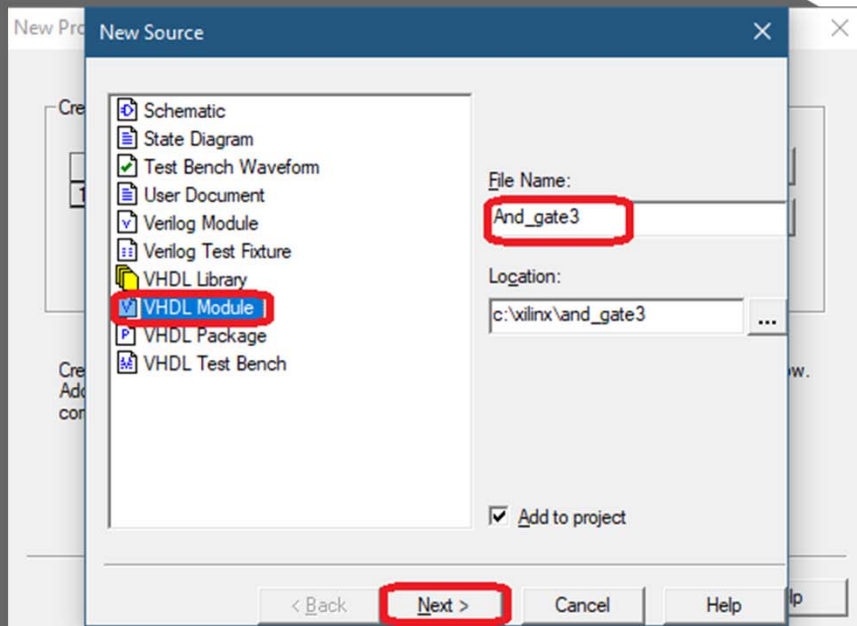
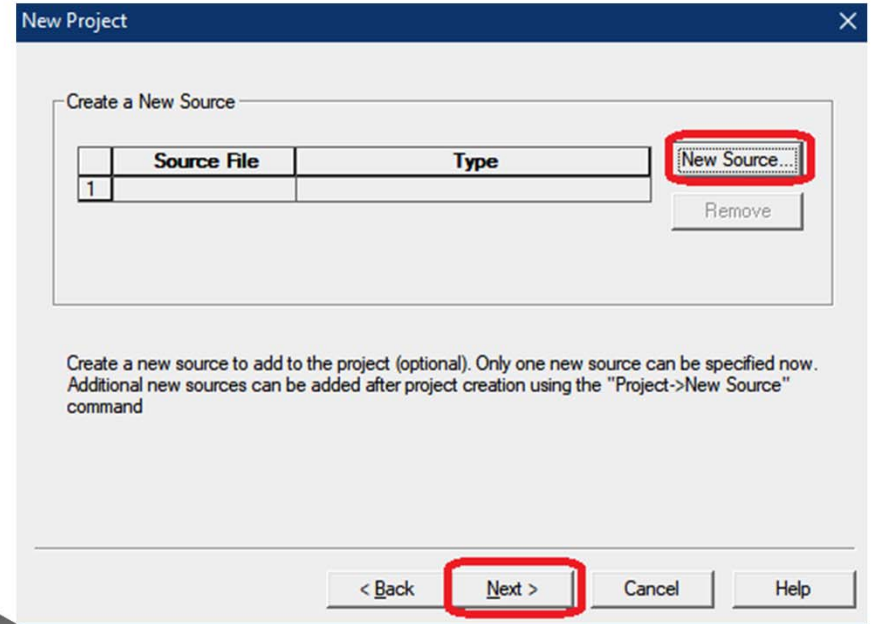
Step3. Write Project name and click Next bottom.

Step4. Select Device Family, Device name, Package and Speed Grade

Click Next bottom

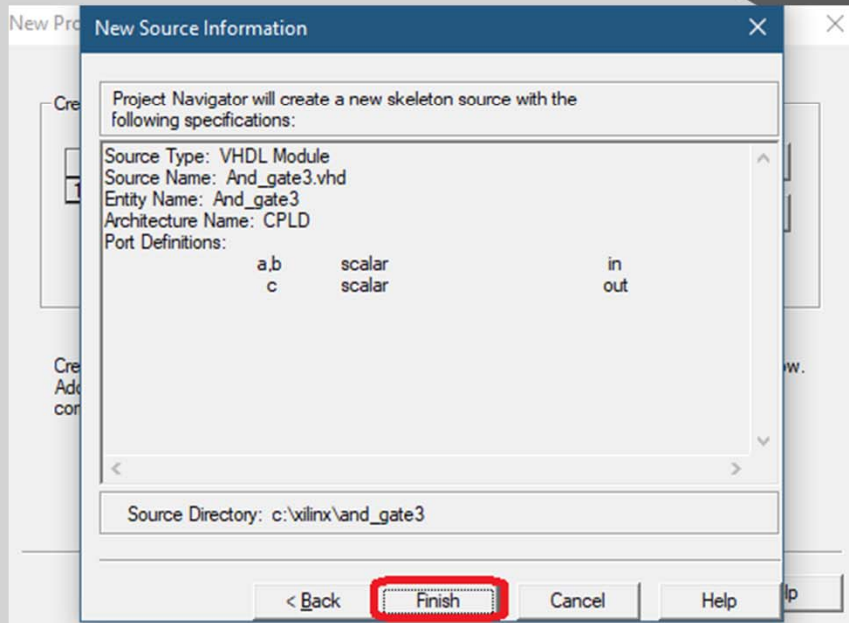
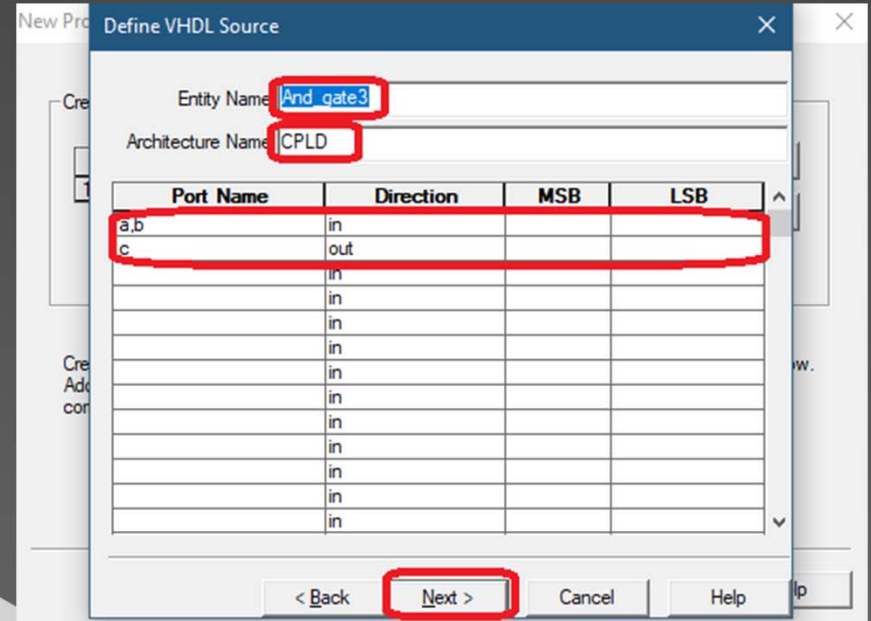


Step5. Add New Source
Step6. Write the File Name As
previous project name
and Select VHDL Module and Click
the Next bottom.

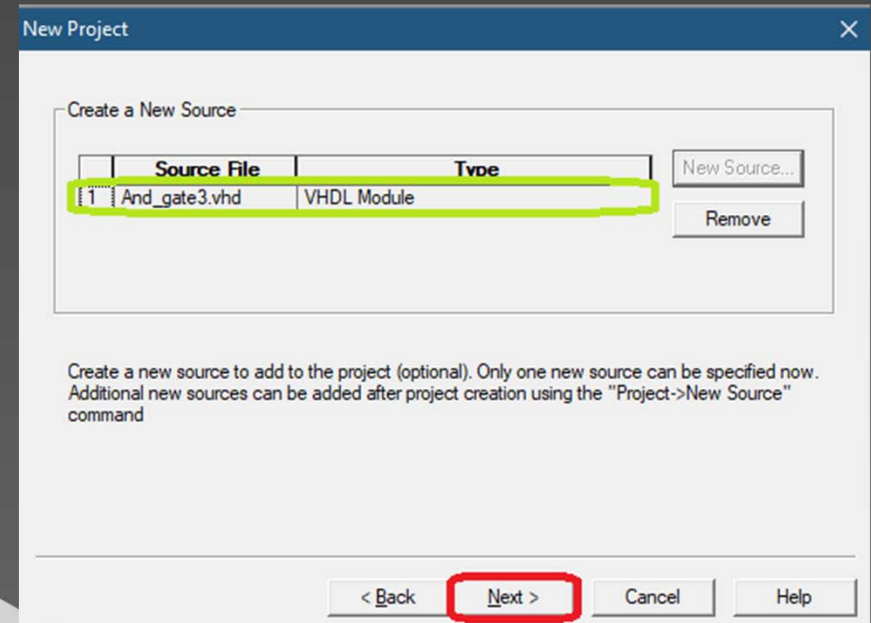
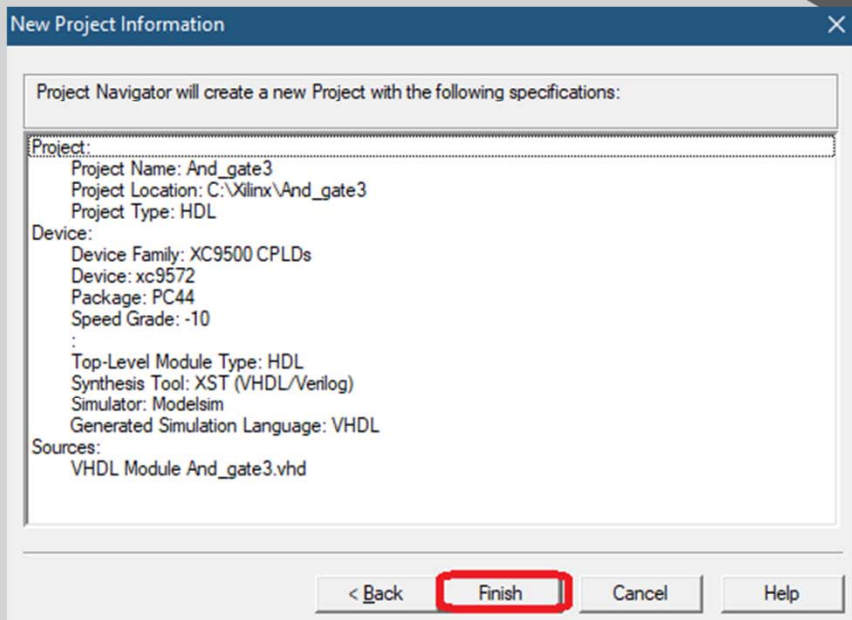


Step7. Write the Architecture Name and Define the Port Name with Direction and Click on Next.

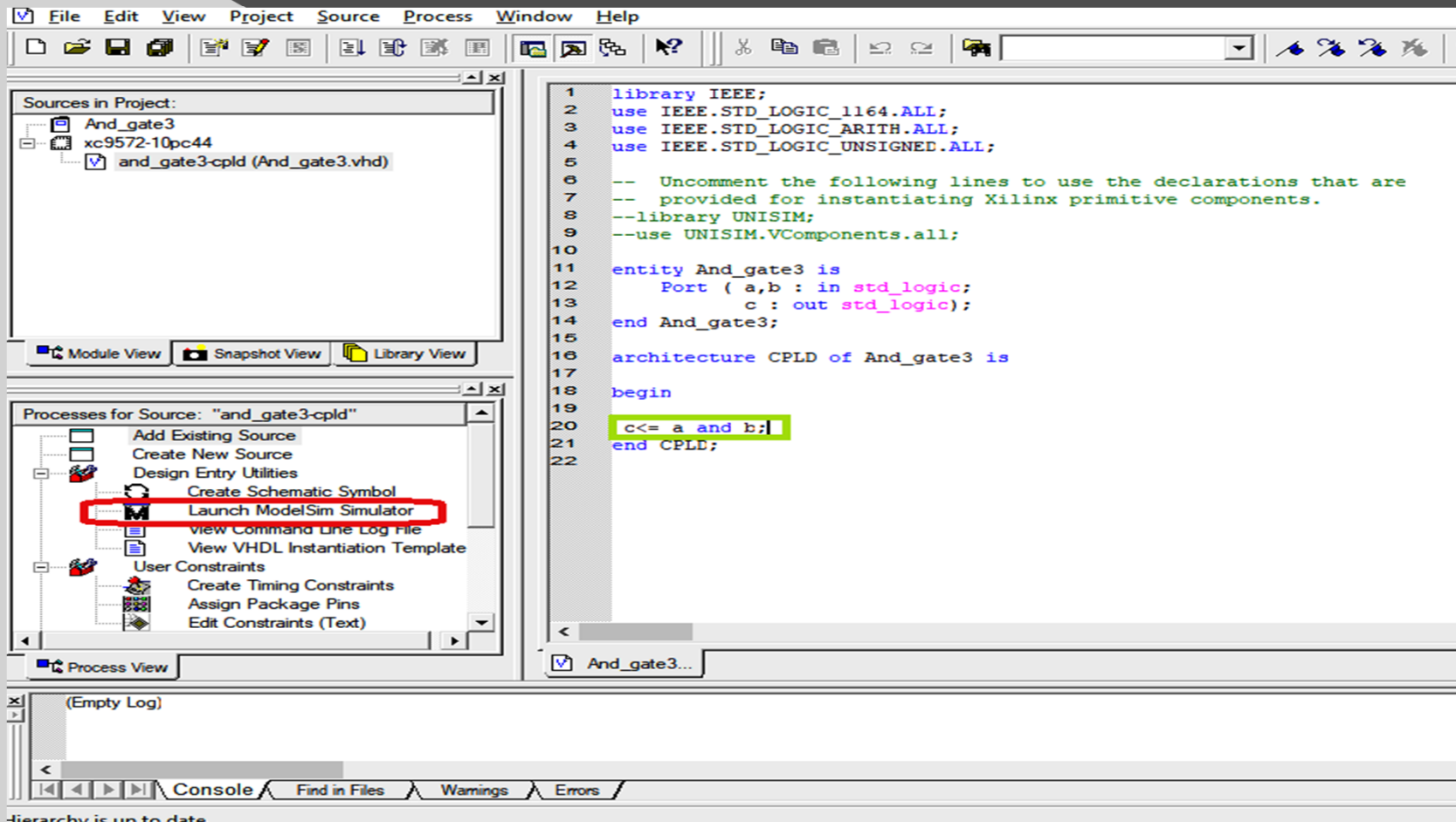
Step8. Click On Finish



Step9. As you can see your file added as Source file after that click on Next
Step10. Click on Finish



Step11. Complete the VHDL Program and Synthesis the design using XST. Click on Lunch ModelSim Simulator.



hierarchy is up to date.

Step12. Put the values and analysis of waveform.

The screenshot displays the ModelSim SE/EE PLUS 5.4a interface during a simulation. The main window shows the simulation progress with a time scale of 100 ns and a delta of 0. The simulation is running on the 'sim:/and_gate3' target.

The **signals** window shows the following signal values:

Signal Name	Value
a	1
b	0
c	0

The **wave - default** window shows the waveform for the signals `/and_gate3/a`, `/and_gate3/b`, and `/and_gate3/c`. The time scale is set to 100 ns, and the current time is 99100 ps to 100100 ps. The waveform shows a constant high signal for 'a' and constant low signals for 'b' and 'c'.

The **Processes for Source: "and_gate3-cpld"** window shows the following processes:

- Add Existing Source
- Create New Source
- Design Entry Utilities
- Create Schematic Symbol
- Launch ModelSim Simulator
- View Command Line Log File
- View VHDL Instantiation Template
- User Constraints
- Create Timing Constraints
- Assign Package Pins
- Edit Constraints (Text)

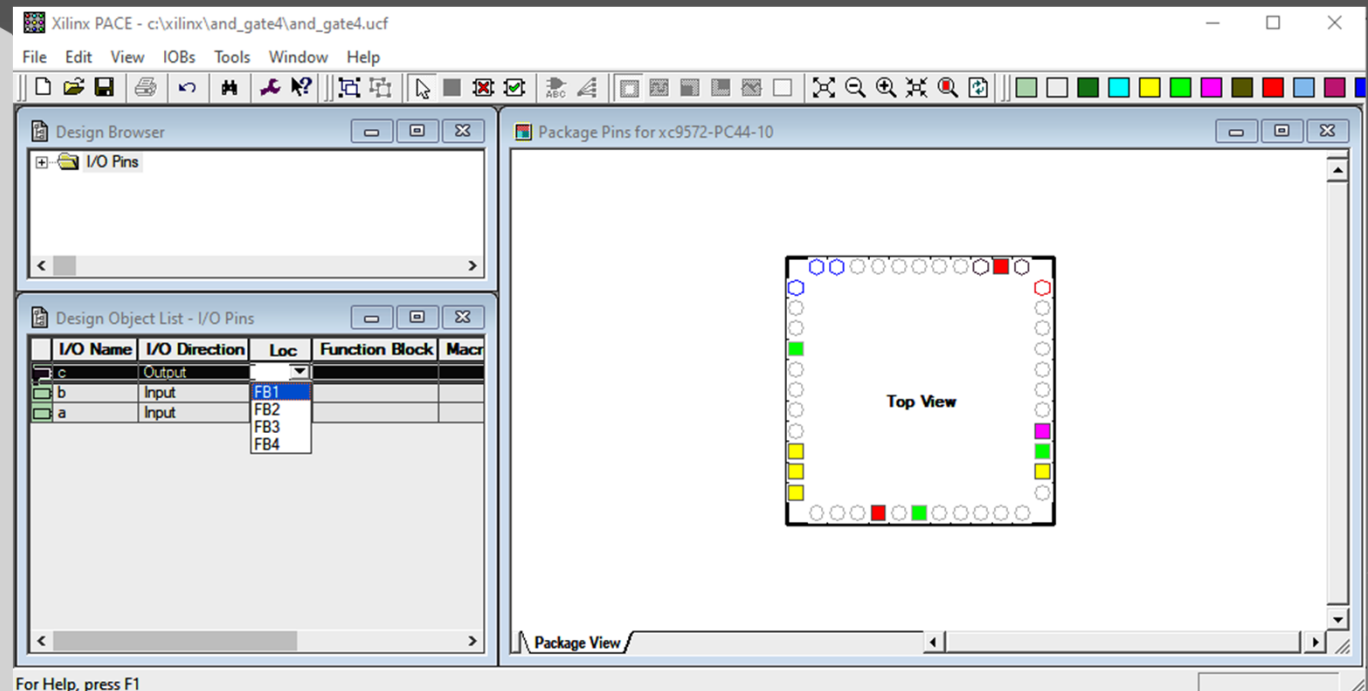
The **Console** window shows the message: "Launching Application for process "Launch ModelSim Simulator"."

Process "L" is up to date.

Ln 20 Col 14

Step13. Analyse the waveform and go to assign pin package bottom. After the connect the CPLD from your computer and burn the program on CPLD.

Now CPLD is ready to use as your respective program.



For Help, press F1

Thanks You