‘Design of combinational circuit using CPLD’

Introduction:

- CPLD stands for Complex Programmable Logic Devices
- CPLD is a programmable logic Device with complexity between that of PALs and FPGAs.
- It is a combination of a fully programmable AND/OR array and a bank of macrocells.
- The AND/OR array is reprogrammable.
- Macrocells are functional blocks that perform combinatorial or sequential logic, and also have the added flexibility for true or complement, along with varied feedback paths.

Pin Diagram:

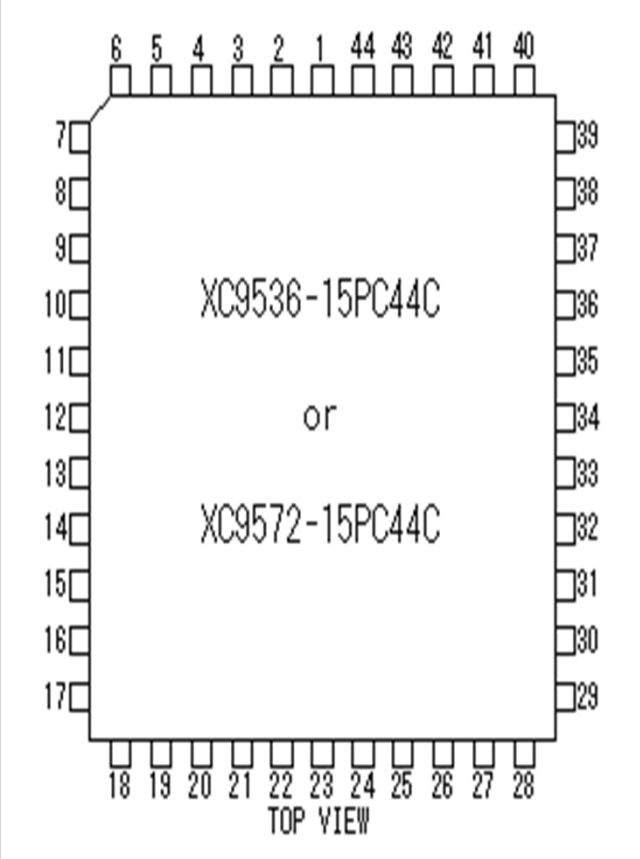


Fig. Pin Diagram of CPLD(XC9572-15PC44C)

Pin No(21,41)= VCC(Dedicated Power Pin)

Pin No(23,31,10)= GND(Dedicated Ground Pin)

Pin No(32)= 3.3v

Pin No(1-9,11-14,18-20,22,24-29,33-40,42-44)= Data Pin(32 Input Pins)

Pin No(15)= TD1(Test Data In, JTAG Pin)

Pin No(16)= TMS(Test Mode Select, JTAG pin)

Pin No(17)= TCK(Test Clock, JTAG Pin)

Pin No(30)= TD0(Test Data Out, JTAG Pin)

Architecture:

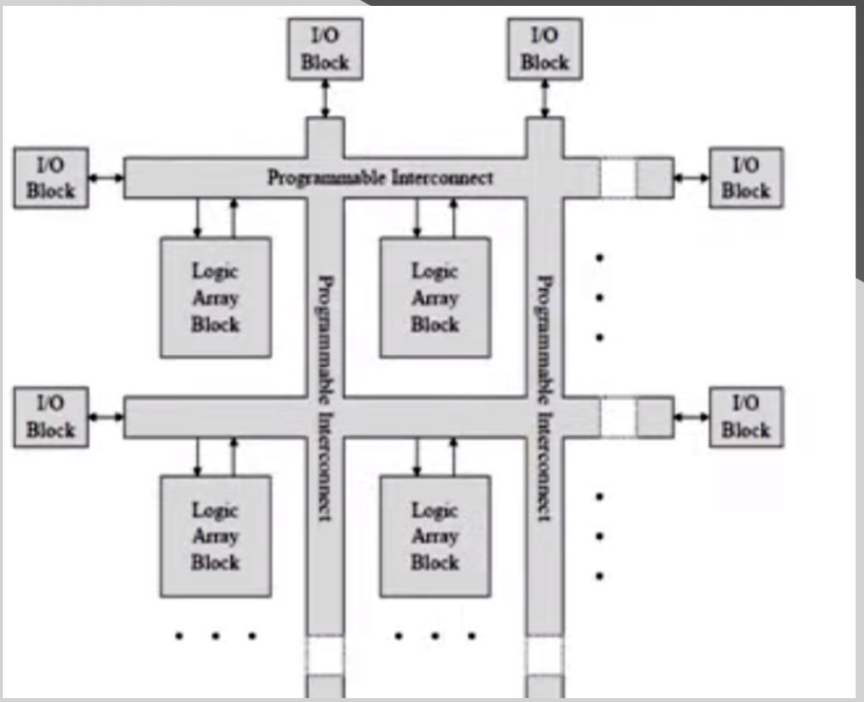


Fig. Architecture of CPLDs

- CPLDs can be use for combinational and sequential logic circuit.
- Logic Array block(LAB) consist 16 marcocells.
- In I/O block, it is a programmable Input and output block for Input, Output and both are.
- Each LAB, memory element and I/O blocks connected with programming interconnect.

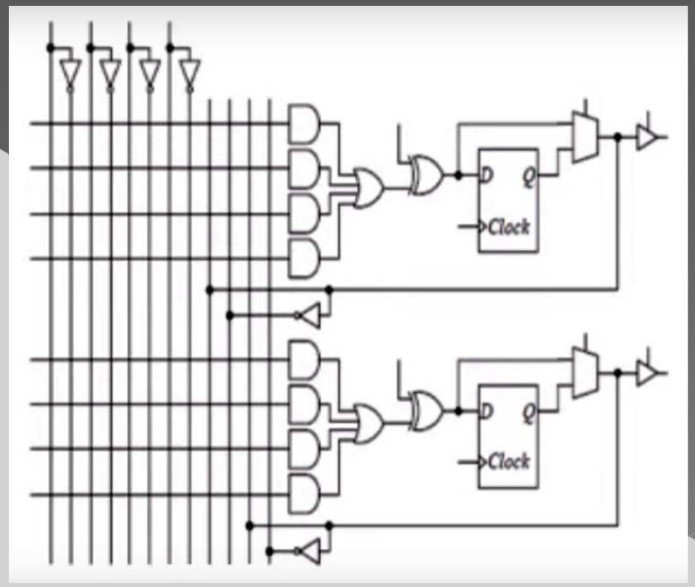


Fig. Logic Diagram of 2 marcocells

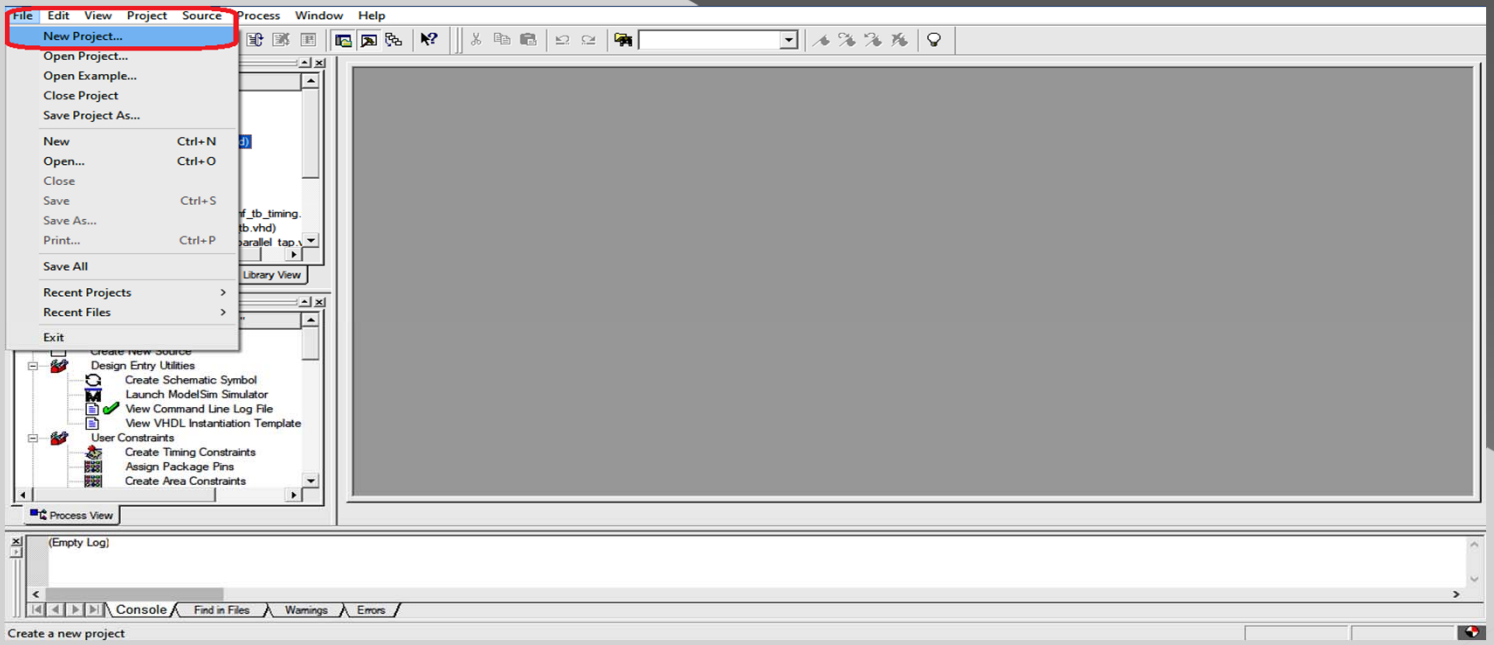
Designing of Combinational Circuit Using CPLDs:

Let's assume we are going to design And Gate using CPLDs.

Here Few Steps to design

Step1.Open Project Navigator which is appear in your Desktop Screen

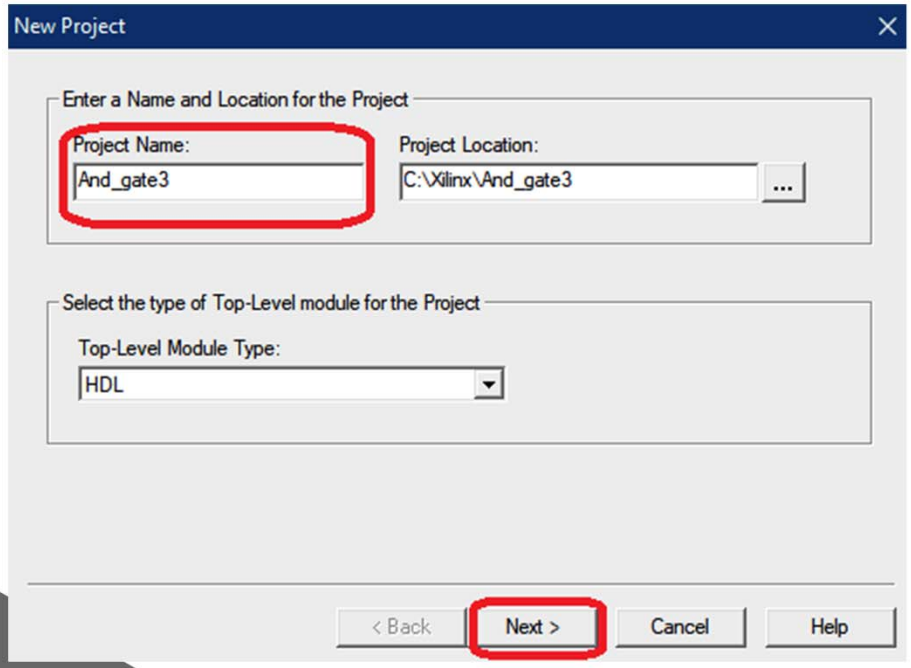
Step2. Go to File and Select New Project.

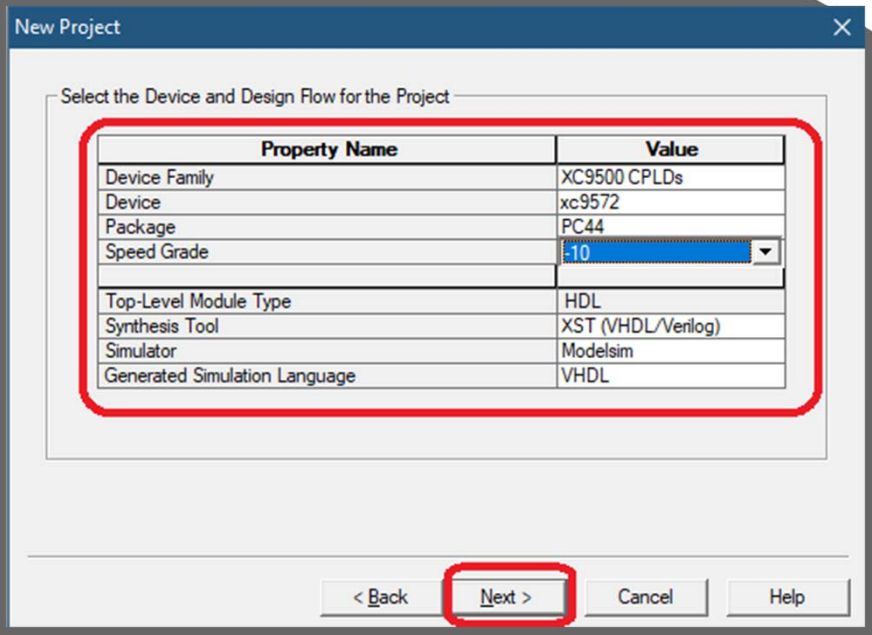


Step3. Write Project name and click Next bottom.

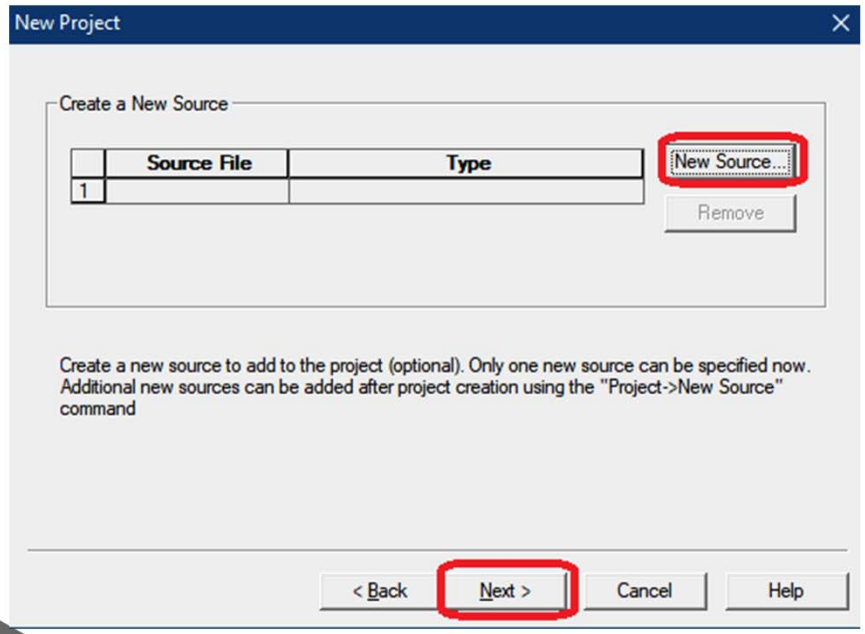
Step4. Select Device Family, Device name, Package and Speed Grade

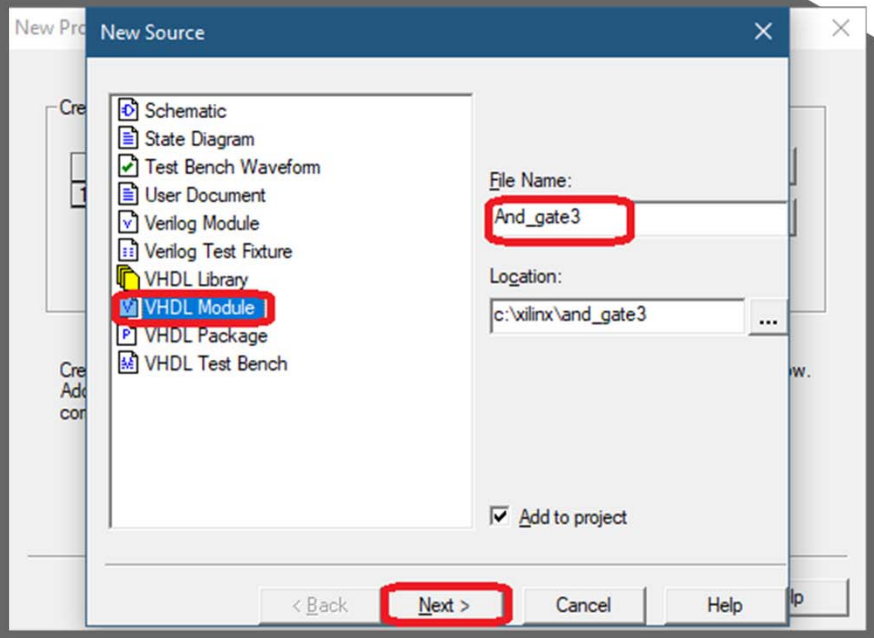
Click Next bottom





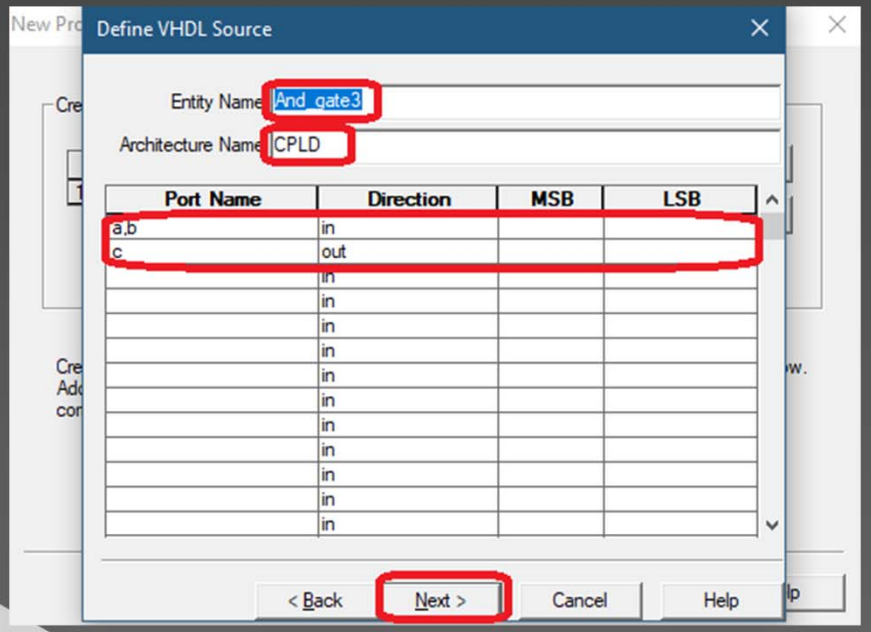
Step5. Add New Source
Step6. Write the File Name As previous project name and Select VHDL Module and Click the Next bottom.

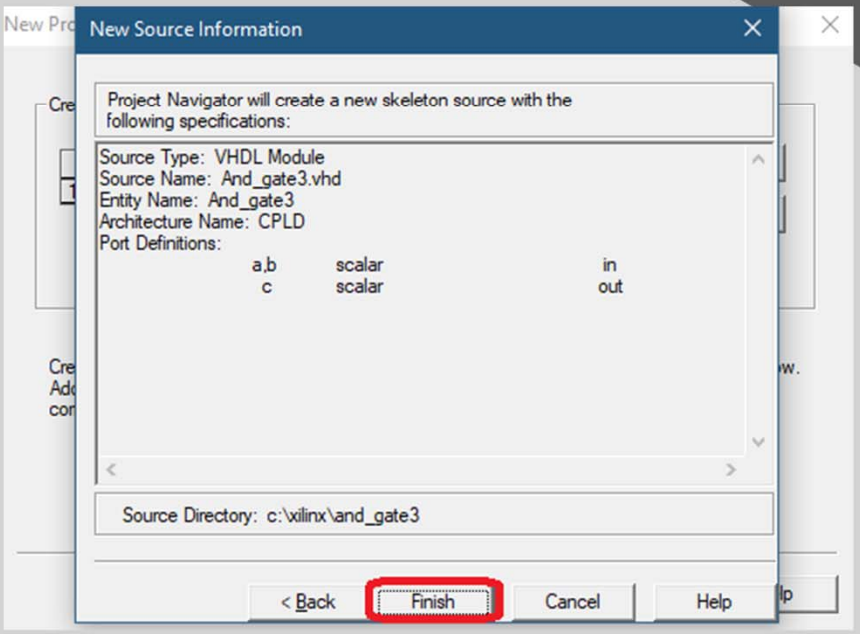




Step7. Write the Architecture Name and Define the Port Name with Direction and Click on Next.

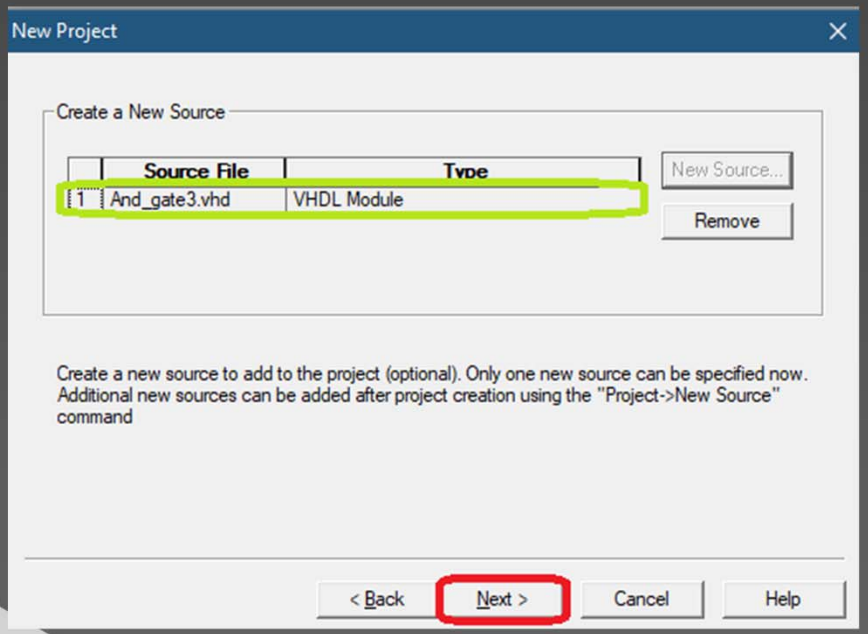
Step8. Click On Finish

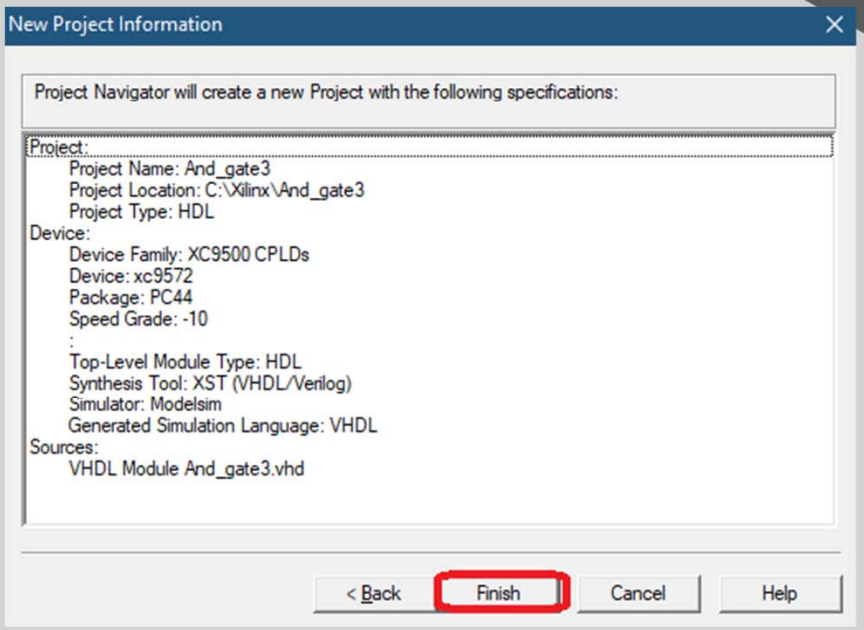




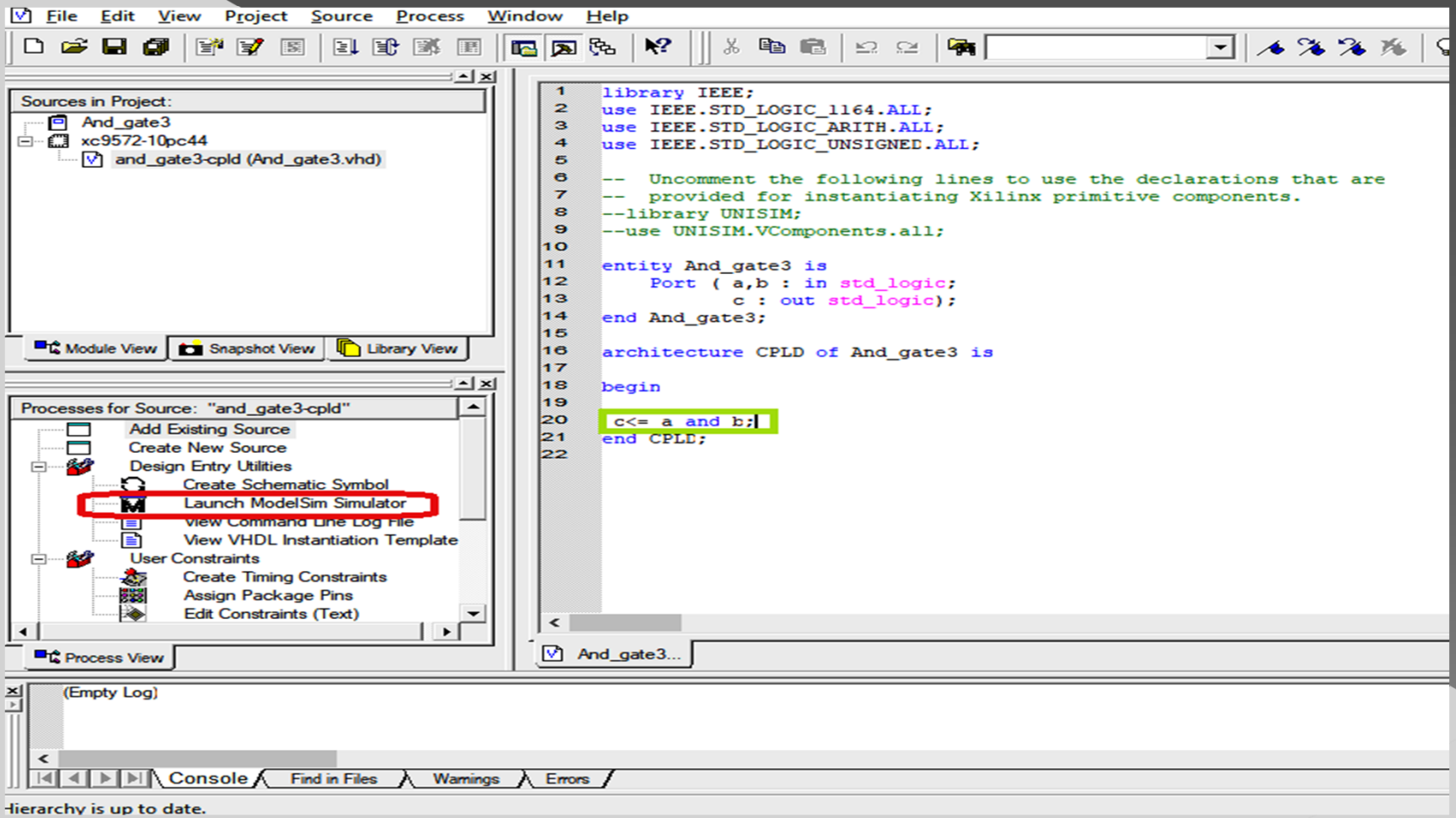
Step9. As you can see your file added as Source file after that click on Next

Step10. Click on Finish

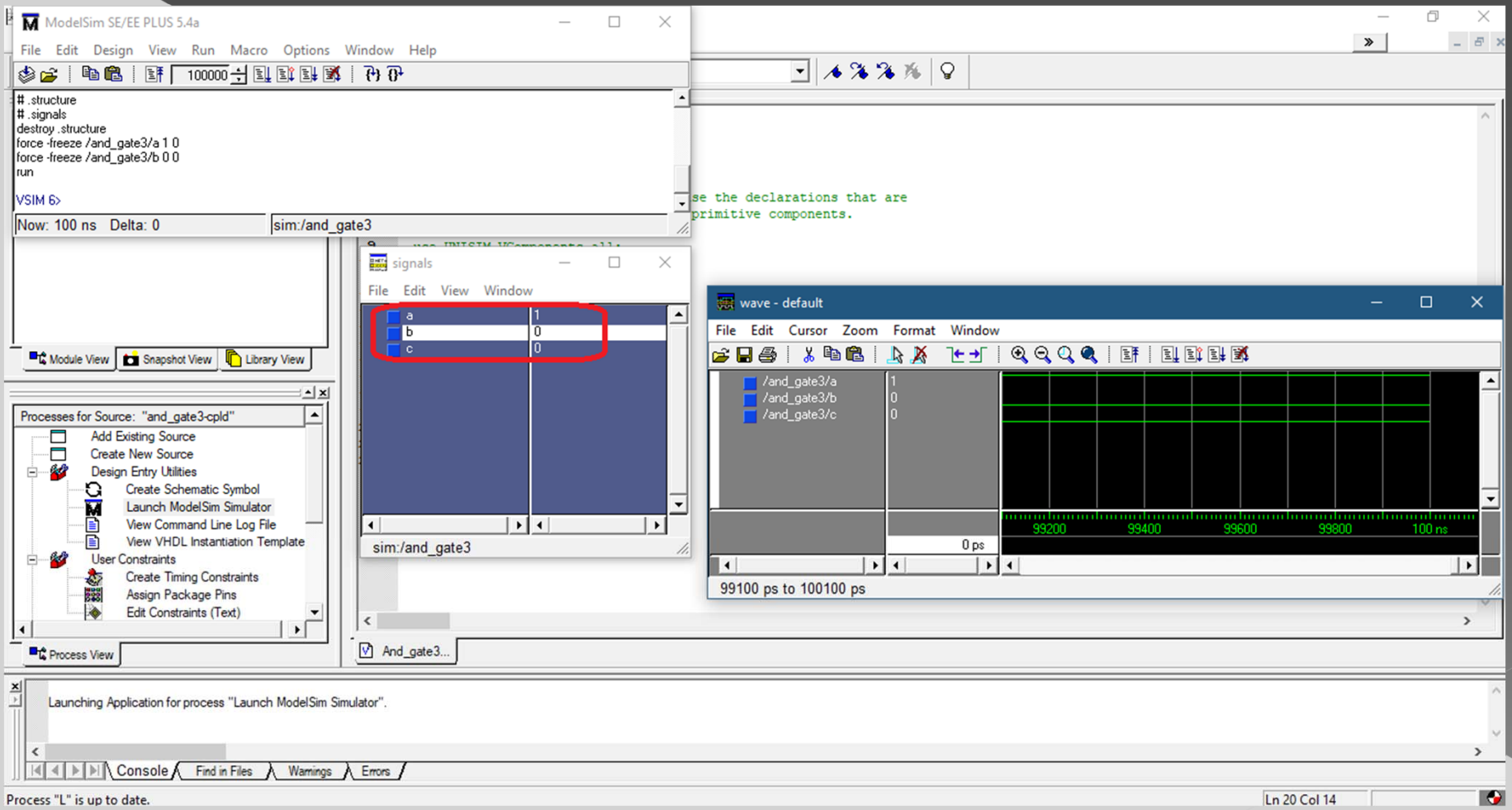




Step11. Complete the VHDL Program and Synthesis the design using XST. Click on Lunch ModelSlim Simulator.

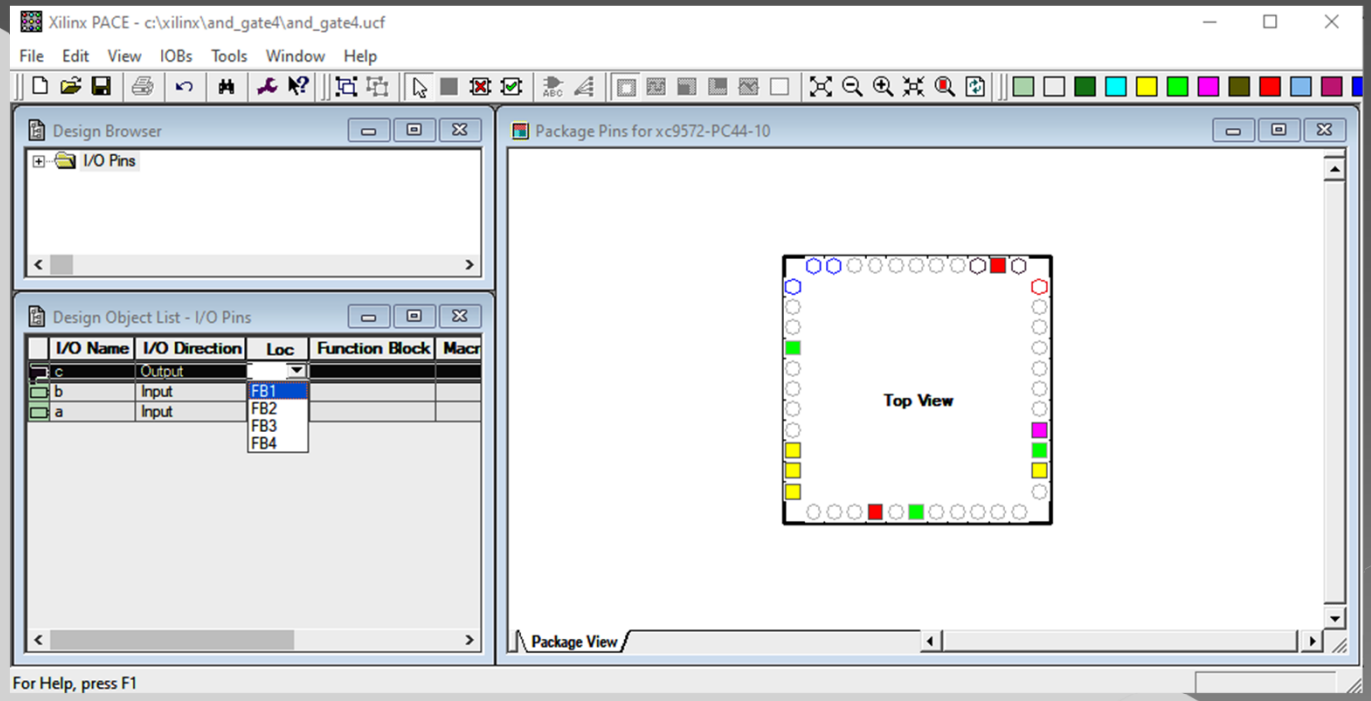


Step12. Put the values and analysis of waveform.



Step13. Analyse the waveform and go to assign pin package bottom. After the connect the CPLD from your computer and burn the program on CPLD.

Now CPLD is ready to use as your respective program.



Thanks You