EnhanceEdu

Types of Delay Models

Delay models

Three types of delay models used in Verilog

- Distributed delay model
- Lumped Delay model
- Pin-to-pin (path) Delay model

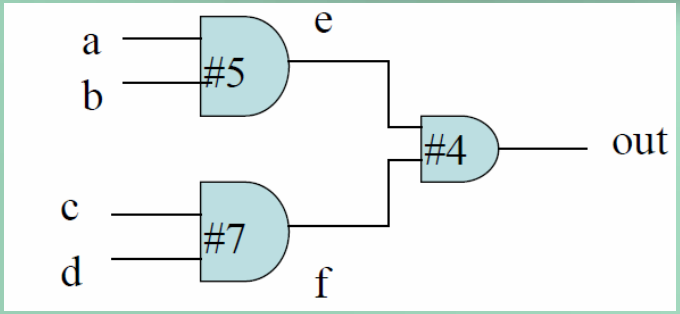
Distributed Delay Model

- Delays that are specified on a *per element basis*
- Distributed delays

a. modelled by assigning delay values - in gate level modelling

b. modelled by assigning delays in the continuous assignment - in data flow modelling

- Provides detailed delay modelling

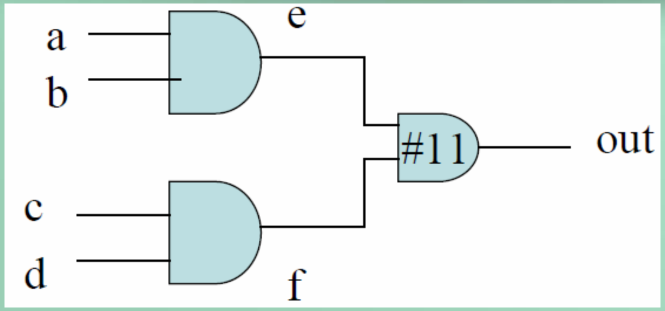



```
module M (out,a,b,c,d);
output out;
input a,b,c,d;
wire e,f;
and #5 a1(e,a,b);
and #7 a2(f,c,d);
and #4 a3(out,e,f);
endmodule
```

```
module M(out,a,b,c,d);
output out;
input a,b,c,d;
wire e,f;
assign #5 e = a & b;
assign #7 f = c & d;
assign #4 out = e & f;
endmodule
```

Lumped delays

- Lumped delays are specified on a *per module basis.*
- Single delay on the output gate of the module – cumulative delays of all paths is lumped at one location.
- They are easy to model compared with distributed delays

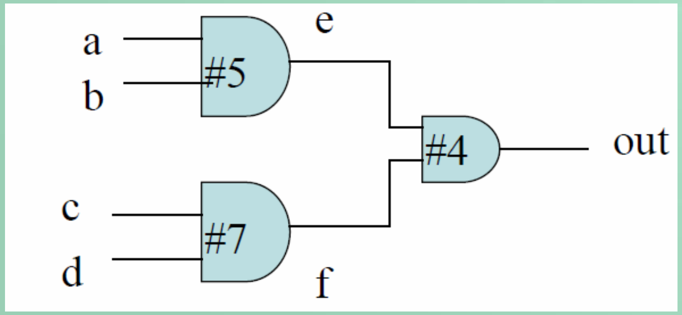



```
module M (out,a,b,c,d);
output out;
input a,b,c,d;
wire e,f;
and a1(e,a,b);
and a2(f,c,d);
and #11 a3(out,e,f);
endmodule
```

```
module M(out,a,b,c,d);
output out;
input a,b,c,d;
wire e,f;
assign e = a & b;
assign f = c & d;
assign #11 out = e & f;
endmodule
```

Pin-to-Pin Delays

- Delays are assigned individually to paths from each input to each output.
- Delays can be separately specified for each input/output path.



- path a-e-out, delay = 9
- path b-e-out, delay = 9
- path c-f-out, delay = 11
- path d-f-out, delay = 11

Path Delays

- Pin-to-Pin delays are named as path delays
- The delay values got directly from Data Books for standard elements.
- For larger Digital Circuits, a low level circuit simulator like SPICE may be used.
- Designer needs to know the I/O pins of the module rather than the internals of the module –so easier to model, even though it is very detailed.

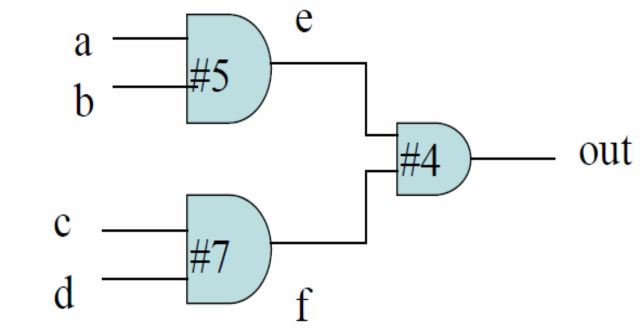
Path Delays

- Distributed Delays and Lumped Delays –already covered.

a. Rise, fall, turnoff delays

b. Min, max, typ delays

- We now study Path Delays
- *Specify blocks*




```
module M (out,a,b,c,d);
output out; input a,b,c,d; wire e,f;
specify
(a => out) = 9;
(b => out) = 9;
(c => out) = 11;
(d => out) = 11;
endspecify
and a1(e,a,b);
and a2(f,c,d);
and a3(out,e,f);
endmodule
```

Specify blocks

- Specify blocks are outside initial and always blocks.
- Inside specify blocks

a. Parallel connections

b. Full connections

c. Conditional Connections

- Parallel: If a[3:0] and out[3:0] are 4-bit vectors then, (a => out) = 9 stands for the shorthand of

```
(a[0] => out[0]) = 9;
(a[1] => out[1]) = 9;
(a[2] => out[2]) = 9;
(a[3] => out[3]) = 9;
```

Specify blocks

- If width does not match for ‘a’ and ‘out’, then it is a illegal connection
- Full Connection: Here every bit in source field connected to every bit of the destination.
- A full connection is denoted by *>
- Example:

```
specify
(a,b *> out) = 9;
(c,d *> out) = 11;
endspecify
```

Conditional Path delays

- specify
- if (a) (a => out) = 9;
- if (~a) (a => out) = 10;
- if (b & c) (b => out) = 9;
- if ((c,d) == 2'b01) (c,d *> out) = 11;
- if ((c,d) != 2'b01) (c,d *> out) = 13;
- endspecify