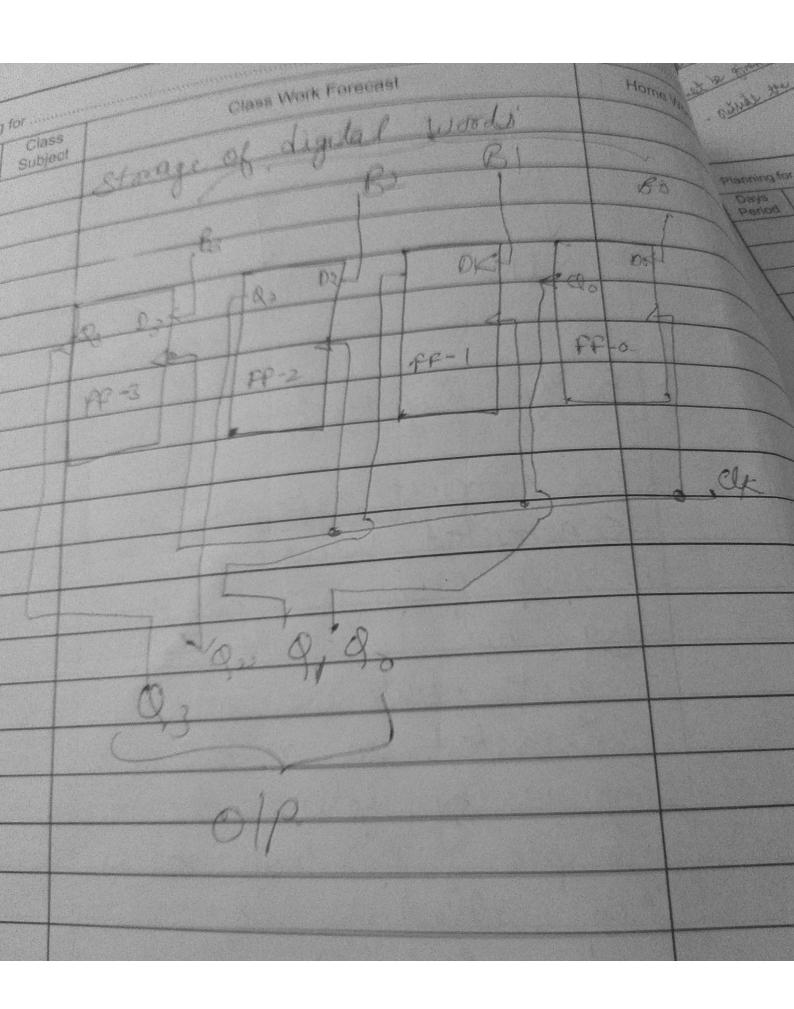
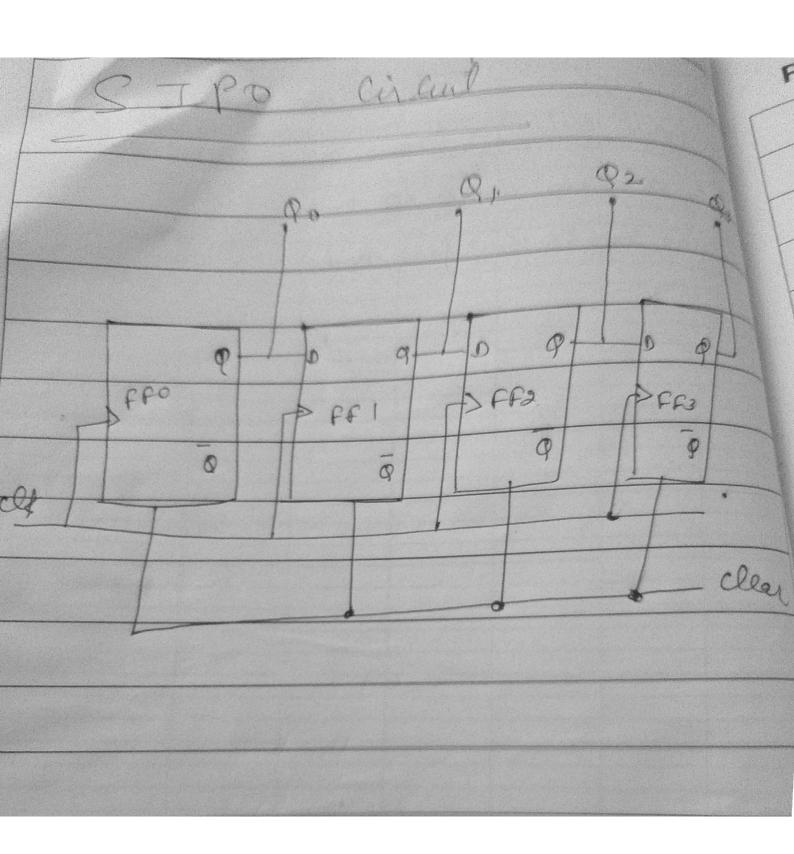
Class Breh 3 1/3 (ECL Cater postop Single - To increase = ops. The "onto my an'n- 61

SIPO Buffer Register : The simplest type of registers
constructed using four.

Deflip floops is shown in f
tig. This is a 4-bit
register, but we can:

constructed on n-bit principle. This register is buffer regisferi In other words the Bu Register are used for temporaly





VHAL Gode for SIPO library ille, use receiste logic\_ 1164. all; entity Sipo W post (Clk, Clear & in std. logic; Input data: in Std\_logic; Q: out std\_logic vector (3 dounts 0)); end Sipo, Architecture behaviour of Sipo 18 begin process (clk). if Clear = "1" then Q <= "00000";

Elsif ( COL' Event and COK = "1") to

A Colombia O <= Q( a dounts o);

B(0) <= Byput\_ Onta;

end process;

end boravious;