

Class Block 3<sup>rd</sup> yrs (ECE)

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Topic: Register

Register: To increase the storage capacity in terms of number of bit we have used a group of flip flop. Such a group of flip flops is known as a register.

\* Thus register is a group of flip flops. The "n-bit" register will consist of "n" number of flip flop and it is capable of storing an "n-bit" word.

Days Period	Class Subject	Class Work Forecast	Home Work
		Registers.	
		↓                      ↓                      ↓	↓
		SISO                      SIPO                      PISO	PIPO

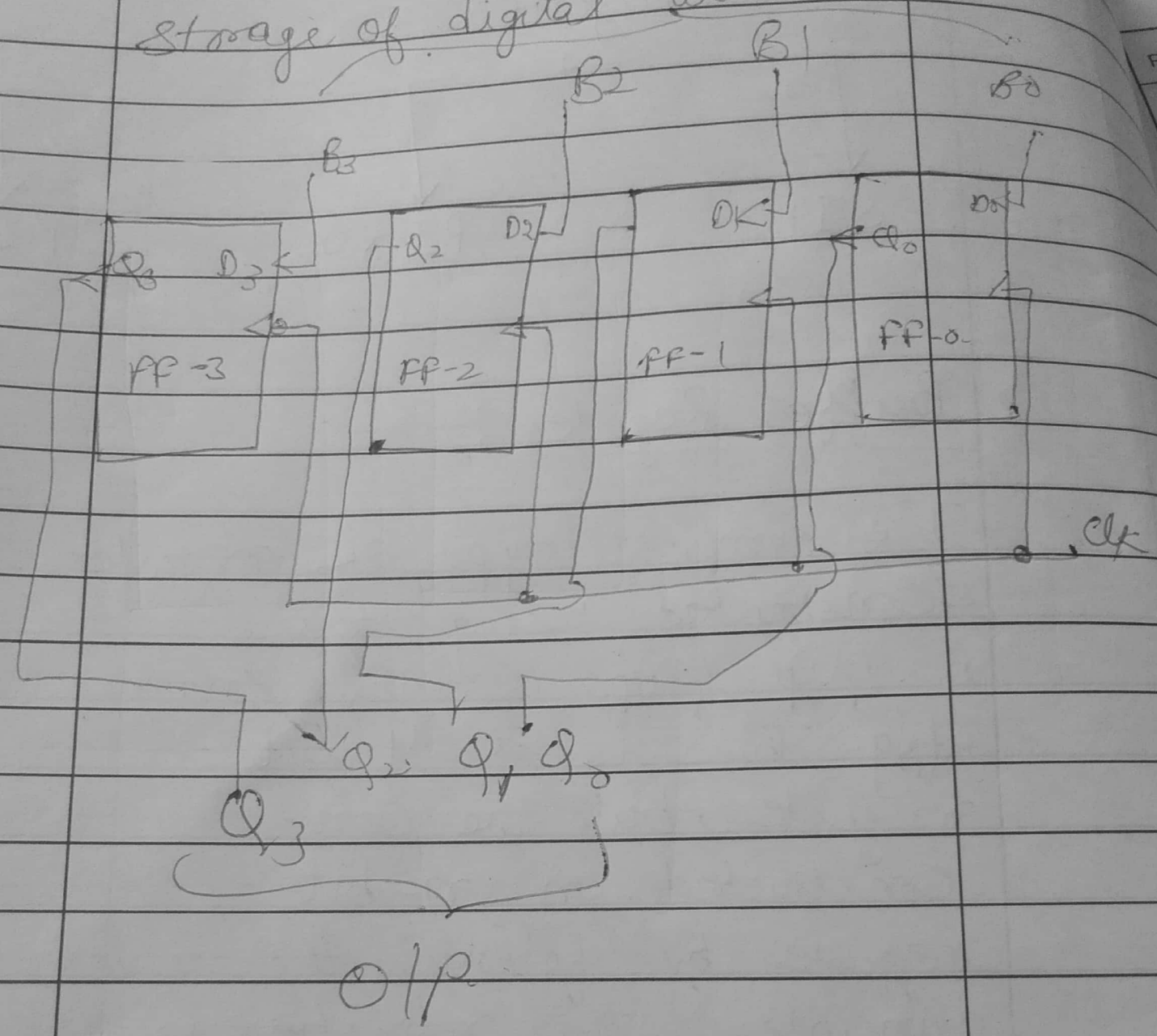
### Buffer Register :-

The simplest type of register constructed using four D-flip flops is shown in fig. This is a 4-bit register, but we can construct an n-bit register by following the same principle. This register is also called as the buffer register.

\*

In other words the Buffer Register are used for temporary

Storage of digital words



Parallel in Parallel out (PIPO):

\* The 4-bit binary DIP  $D_0, D_1, D_2, D_3$  is applied to the data DIP  $D_0, D_1, D_2$  and  $D_3$  respectively of the four flip-flops.

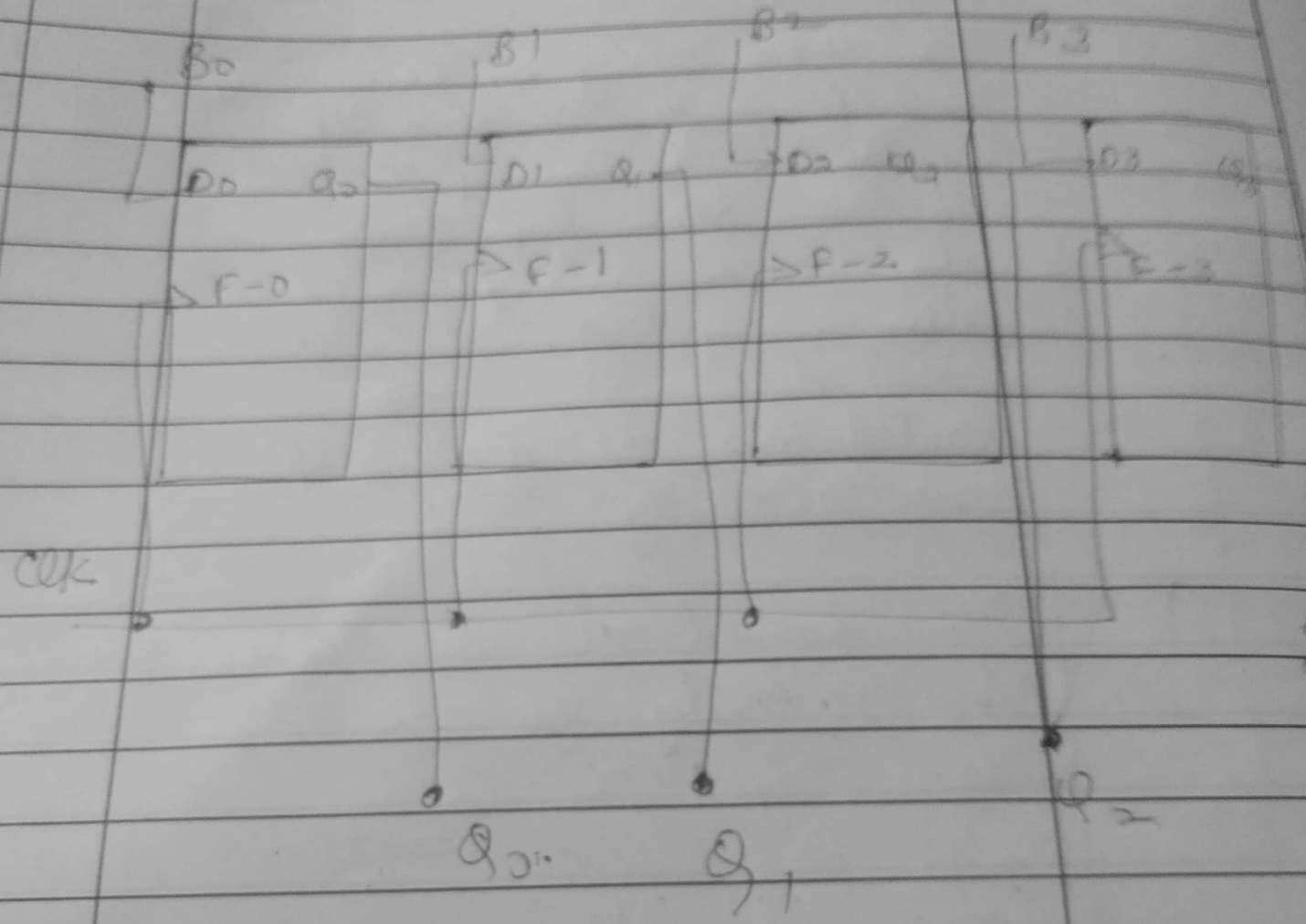
\* As soon as a negative clock edge is applied, the DIP binary data will be ~~ads~~ loaded into the flip flops simultaneously.

\* The loaded data will appear simultaneously to the DIP side. Only one clock pulse is essential to load all bits.

Planning for ..... to .....

Days Period	Class Subject	Class Work Forecast	Home Work
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4 Bit Parallel data I/P



Parallel O/P



Verilog code for PIPO;

```
library ieee;
use ieee.std_logic_1164.all;
```

```
entity PIPO is
port (
```

```
    clk : in std_logic;
```

```
    D : in std_logic_vector (3 downto 0);
```

```
    Q : out std_logic_vector (3 downto 0));
```

```
end PIPO;
```

Architecture Behaviour of PIPO is

```
begin
```

```
    process (clk)
```

```
    begin
```

Period	Class Subject	Class Work Forecast
		if (clk'event and clk = '1')
		then
		$Q \leq D;$
		end if;
		end process;
		end Behaviour;