Days Period | Class Subject | Class Work Forecast | Home Work

Class - B.Tech 3rd yr (ECE)
Subject :- ADDV.
Faculty :- Mandeep Singh
Date :- 7/5/2020

Topic :- Design of 4Bit Down Counter

Q: VHDL Code for a 4-Bit Down Counter.

Ans:-
```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity dcounter is
port (clock, clr : in std_logic;
      q : out std_logic_vector (3 downto 0));
end dcounter;
```

Class Work Forecast ..... to .....

Home Work

Architecture Behaviour of dcounter is

Signal tmp : std_logic_vector (3 downto 0);

begin

process (clock, clr)

begin

if (clr = '1') then

tmp <= "1111" ~~then~~

elsif (clock'event and clock='1') then

tmp <= tmp - 1;

end if;

end process;

Q <= tmp;

end behaviour;

Planning for .... to ....

Days Period	Class Subject	Class Work Forecast					Home Work
						State	Decimal Equivalent
	Clk	flip flop o/p					
		Q_D	Q_C	Q_B	Q_A		
	Initially	0	0	0	0	1	0
	1(↓)	1	1	1	1	2	15
	2(↓)	1	1	1	0	3	14
	3(↓)	1	1	0	1	4	13
	4(↓)	1	1	0	0	5	12
	⋮	⋮	⋮		⋮	⋮	⋮
	15(↓)	0	0	1	0	15	2
	16(↓)	0	0	0	1	16	1
	1(↓)	0	0	0	0	1	0
	2(↓)	1	1	1	1	2	15

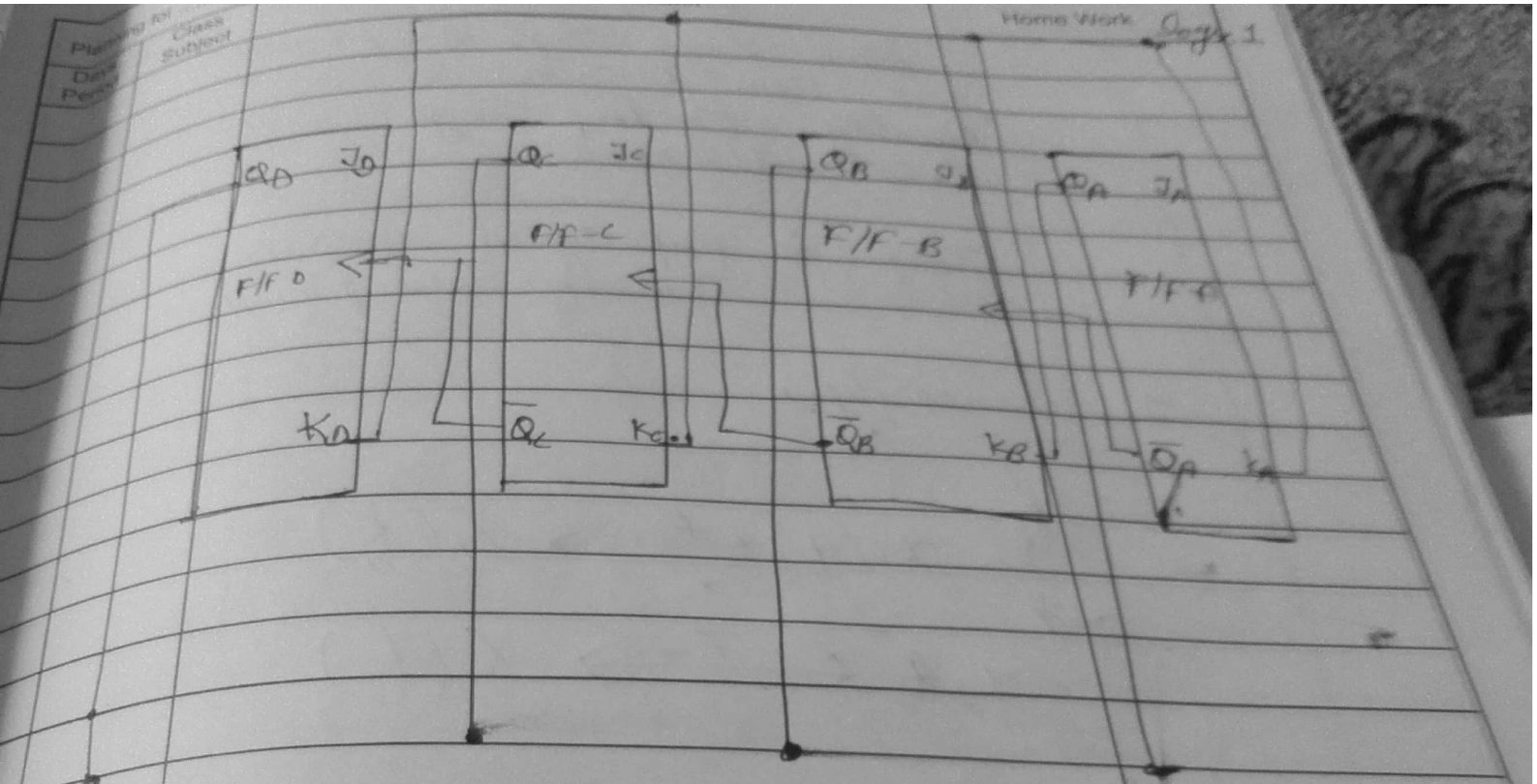

Fig: 4 Bit Asynchronous Counter

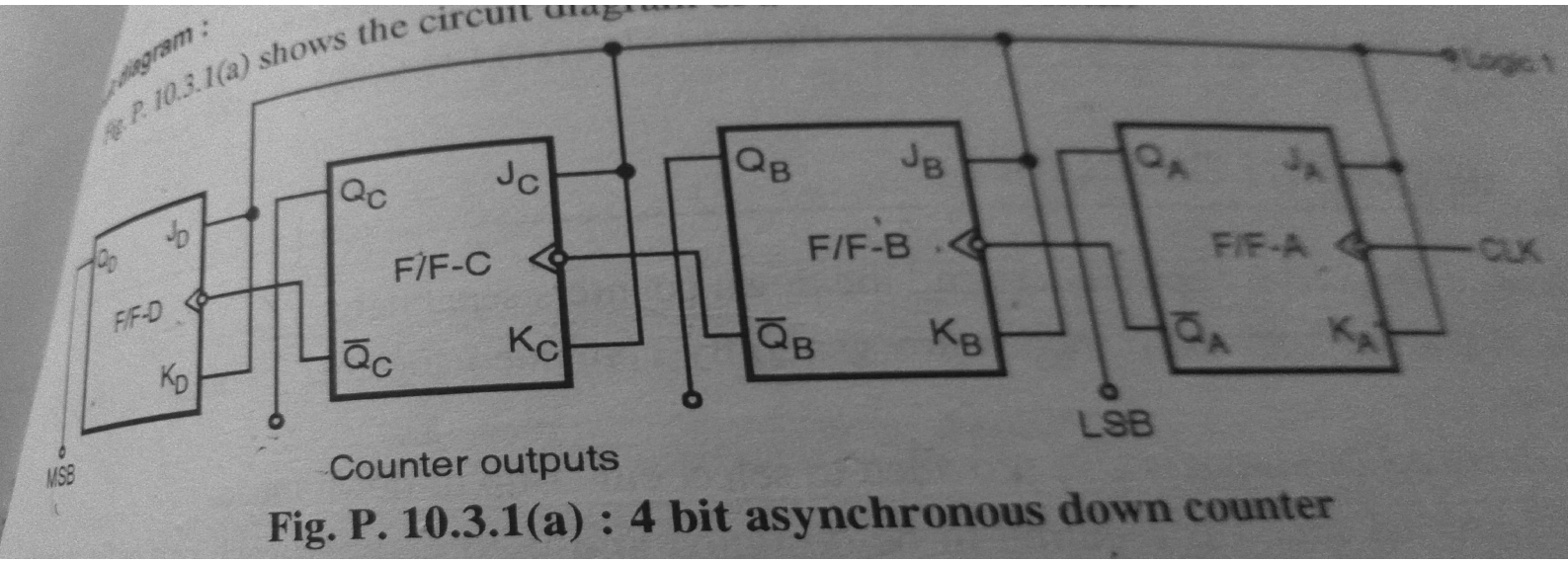

Fig. P. 10.3.1(a) : 4 bit asynchronous down counter