Class- B.Tech 3rd yr ECE
Sub: ADDV
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Topic: T- flip flop

Q. Design of T- flip flop

Ans:
```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity Toggle_flip_flop is
    Port ( t : in std_logic;
           clk : in std_logic;
           reset : in std_logic;
           dout : out std_logic );
end Toggle_flip_flop;
```

Architecture behaviour of Toggle_flip_flop

begin

tff : process (t, clk, reset) is

Variable m: Std_logic := '0';

begin

if (reset = '1') then

m := '0';

elsif (rising_edge (clk) then

```
if (t = '1') then
xn := not xn;
end if;
dout <= xn;
end process tff;
end behaviour;
```

Input		output	
T	clk	Q_n	$\overline{Q_n}$
0	X	Q_n	$\overline{Q_n}$
1	↑	Q_n	$\overline{Q_n}$
1	0	Q_n	$\overline{Q_n}$
1	1	Q_n	$\overline{Q_n}$
1	↓	$\overline{Q_n}$	Q_n