class - B.tech 3rd yr ECE
Subject : ADDV
Faculty : Mandeep Singh
Date : 1/5/2020

Topic :- Design of Synchronous circuit

① Design of SR Latch.

Ans :-

```
library ieee;
use ieee.std_logic_1164.all;

entity srl is
port ( r, s : in bit;
       q, qbar : buffer bit);
end srl;
```

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```
Architecture behaviour of srl is
Signal s1, r1 : bit;
begin

  q <= s nand qbar;

  qbar <= r nand q;

end behaviour;
```

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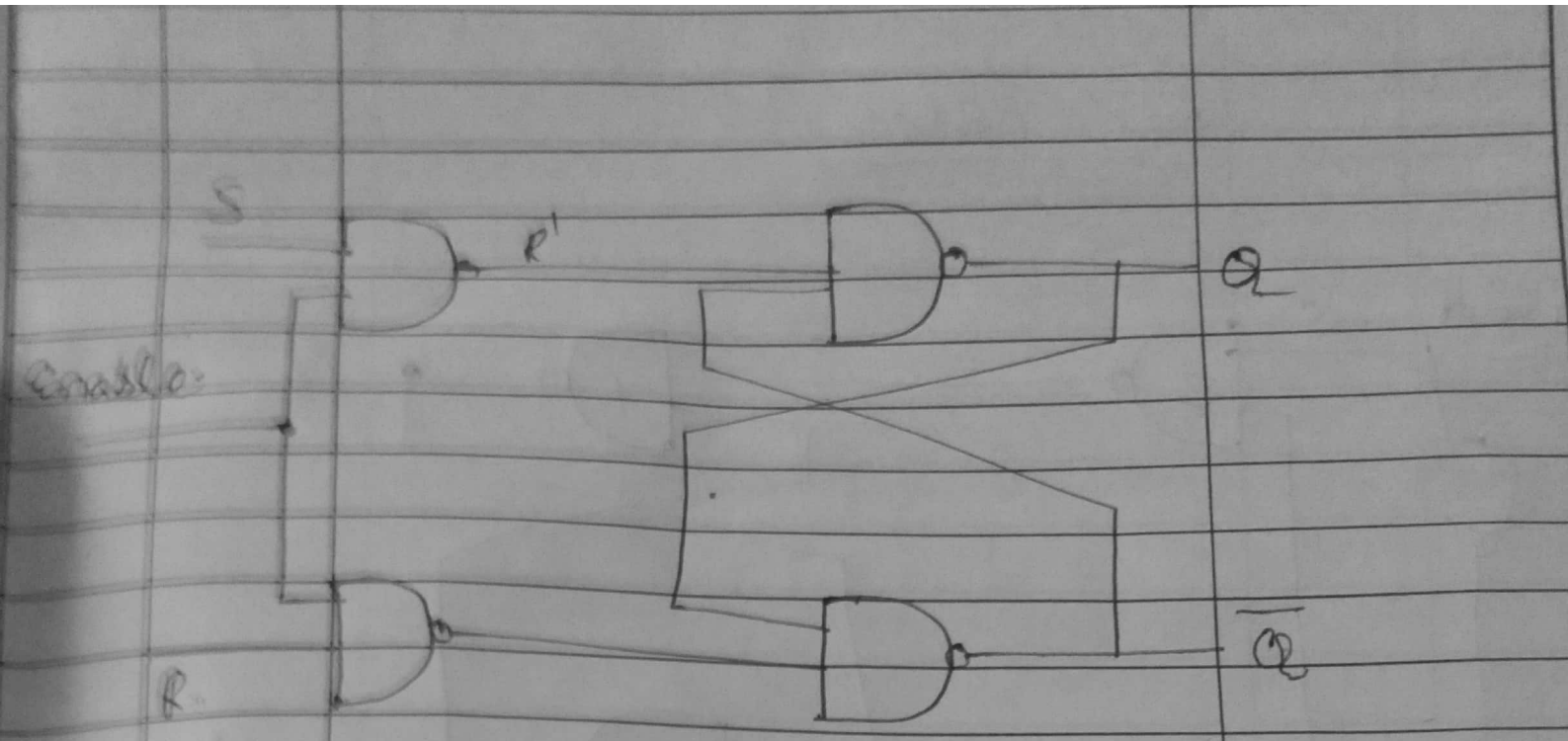

E	S	R	Q_n	$\bar{Q}$
0	X	X	Q_n	$\bar{Q}$
1	0	0	Q_n	$\bar{Q}$
1	0	1	0	1
1	1	0	1	0
1	1	1	Intermediate	

Remarks :

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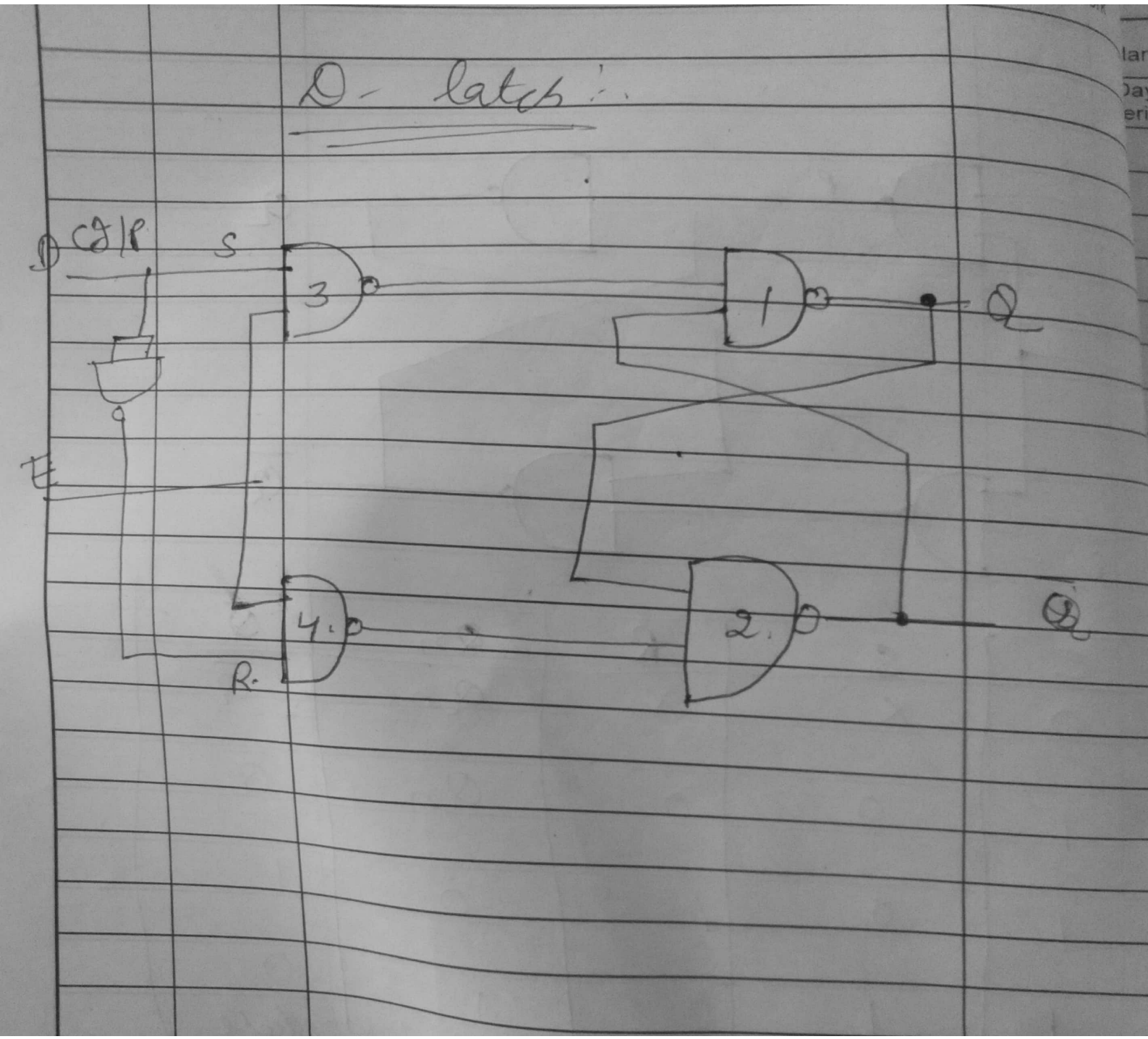
D- latch :



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I/P		Output	
E	D.	Q_n	$\overline{Q_n}$
0	X.	Q_n	$\overline{Q_n}$
1	0	0	1
1	1	1	0

Truth table

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Planning for ..... to .....

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VHDL Code for D latch,

```
library ieee;
use ieee.std_logic_1164.all;

entity D1 is
    port(d : in bit;
         q, qbar : buffer bit);

end D1;

Architecture behaviour of D1 is
Signal S1, R1 : bit;
begin
```

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```
q <= d nand qbar;
qbar <= d nand q;
end behaviour;
```

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