Class Work Forecast | Home Work

class - B.Tech (E C E) 3rd yr.
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Topic: Design of 4-Bit Up/Down Counter

```
library IEEE;
use ieee.std_logic_1164.All;

entity tbCounter is
Port ( clk: in std_logic;
       reset: in std_logic;
       up_down: in std_logic;
       Counter: out std_logic_vector
                (3 downto 0));
end tbCounter;
```

```
Architecture Behaviour of tbcounter is
Signal counter_updown : std_logic_vector (3 downto 0);
begin
  process (clk, reset)
    begin
  if (rising_edge (clk)) then
  if (reset = '1') then
        Counter_updown <= "0";
elsif (up_down = '1') then
      Counter_updown <= "1";
else
```

```
Counter_updown <= "1";
    end if;
end process;
Counter <= Counter_updown;
    end Behavioural;
```

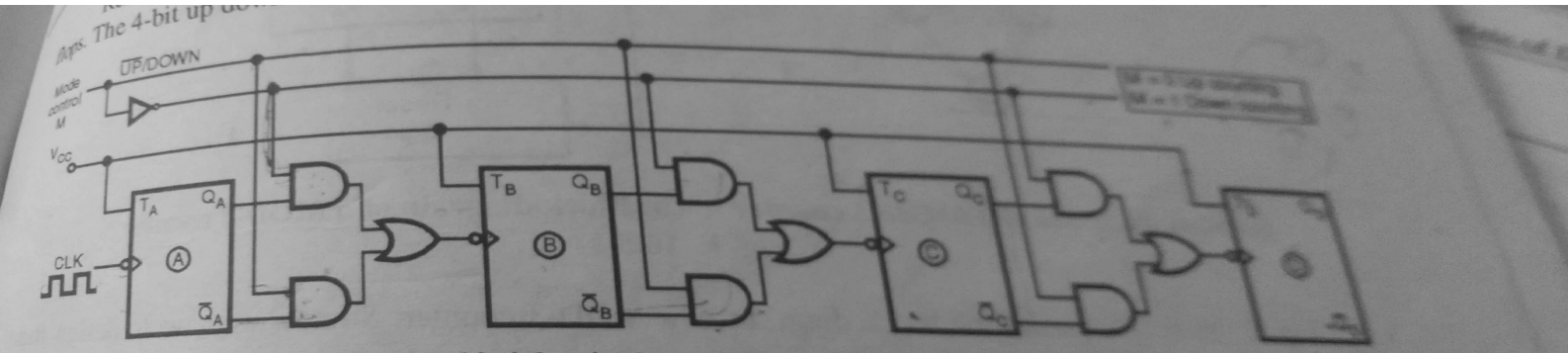

Fig. P. 10.4.2 : 4-bit up/down ripple counter

The circuit will work as up counter with M = 0 whereas it will operate as a down counter when M = 1.