Class Work

Home Work

class - B.Tech (ECE) 3rd yr.

Sub : ADDV

Faculty : Mandeep Singh

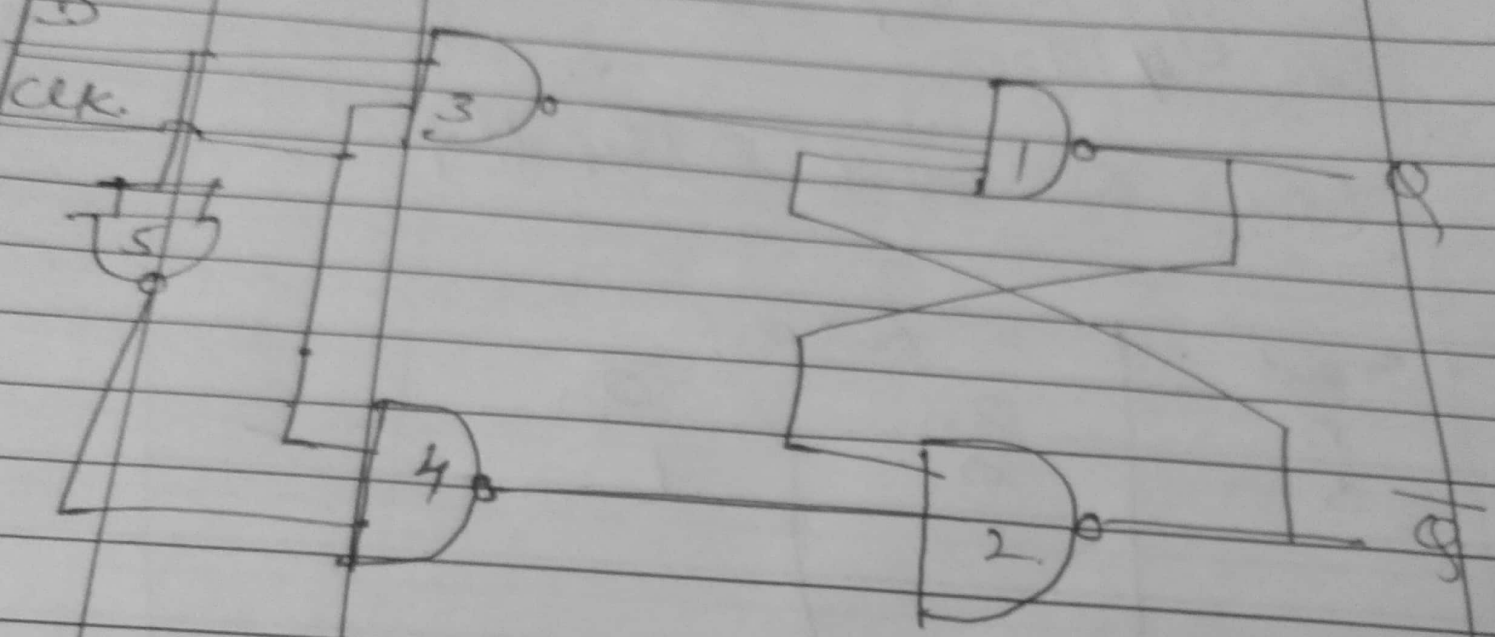
Date : 19/5/2020

Topic : Design of D flip flop

Input		Output	
clk	D	Q_n	$\overline{Q_n}$
↑	0	0	1
↑	1	1	0

Planning for ..... to .....

Days Period	Class Subject	Class Work Forecast	Home Work



VHDL Code for D flip flop:

```
library ieee;
use ieee.std_logic_1164.all;

entity dff is
port (d, clk : in bit,
      q, qbar : buffer bit);
end dff;

Architecture of Dff is
signal d1, d2 : bit;
begin
```

```
dK <= d rand clk;
d2 <= (not d) rand clk;
q <= d1 rand qbar;
qbar <= d2 rand q;
end behaviour
```