Class Work Forecast

Class B.Tech 3rd yr (ECE)
Subt ADDV
Faculty: Mandeep singh
Date: 2/5/2020

Topic: Design of flip flop

Q.1. Design of JK flip flop:

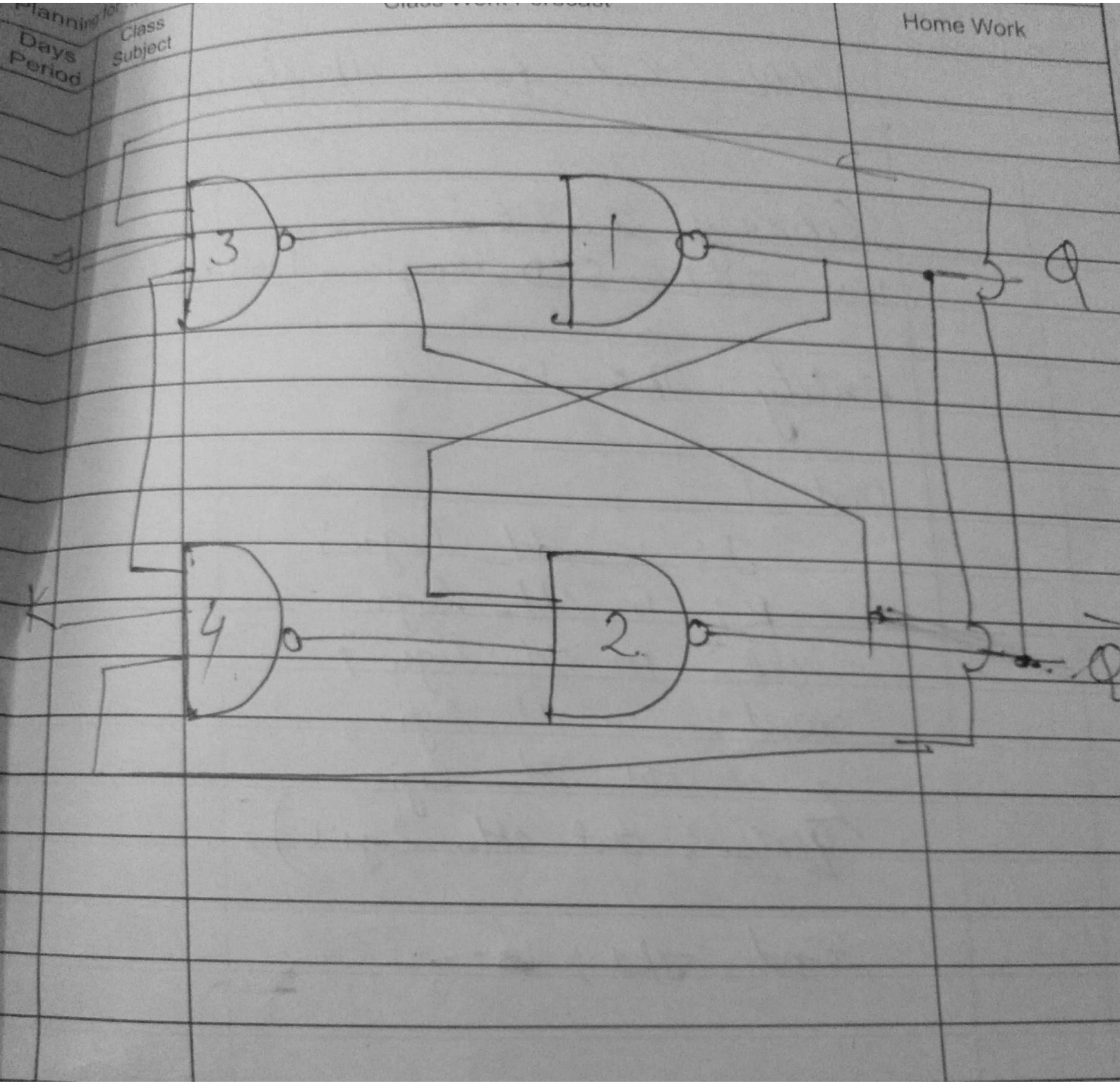
Inputs			Outputs	
E	J	K	Q_n	$\overline{Q_n}$
0	X	X	Q_n	$\overline{Q_n}$
1	0	0	Q_n	$\overline{Q_n}$
1	0	1	0	1
1	1	0	1	0
1	1	1	$\overline{Q_n}$	Q_n

Planning for

Days
Period

Class
Subject

Home Work



VHDL - Code for a JK flip flop

```
library IEEE;
use IEEE.STD_Logic_1164.all;

entity JK1 is

port (
      J: in std_logic;
      K: in std_logic;
      clk: in std_logic;
      reset: in std_logic;
      q: out std_logic;
      qbar: out std_logic);

End JK1;
```

to

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```
architecture behaviour of JK is
begin
JK1 : process (J, K, clk, reset) is
variable m : std_logic := '0';
begin
if (reset = '1') then
    m := '0';
elsif (rising_edge (clk)) then
    if (J = K) then
        m := J;
    elsif (J = '1' and K = '1')
        m := not m;
    end if;
```

q <= xn;

qb <= not xn;

end process ∃k1;

end behaviour;