Class- B.Tech 3rd year
Subj- ADDA
Faculty- Mandeep Singh
Date 7/4/2017

CPLD (Complex Programmable logic Device):-
Using Rom, PLA, PAL to implement a Combo circuit is fairly straightforward and easy to do. These devices can be used to implement the circuits that do not require more no. of I/P, O/P product terms that are provided in a chip. These chips are limited to fairly modest size typically supporting a combinational no. of I/P plus O/P of not more then 32. However to implement a sequential circuit or a more complex combinational circuit may require more sophisticated and larger programming device. The CPLD is capable to implement a ckt with upward 10,000 logic gate and logic capacity upto 90 single SPLD.
Xilinx the world largest manufacturer of programmable semiconductor introduces two main families XC4000 and XC9500. offering the 7200 series originally marked as the logic and the Super EPLD and 7300 developed by Xilinx

2.2.5 PIN OUT DIAGRAM OF CPLD (XC9572-15PC4)

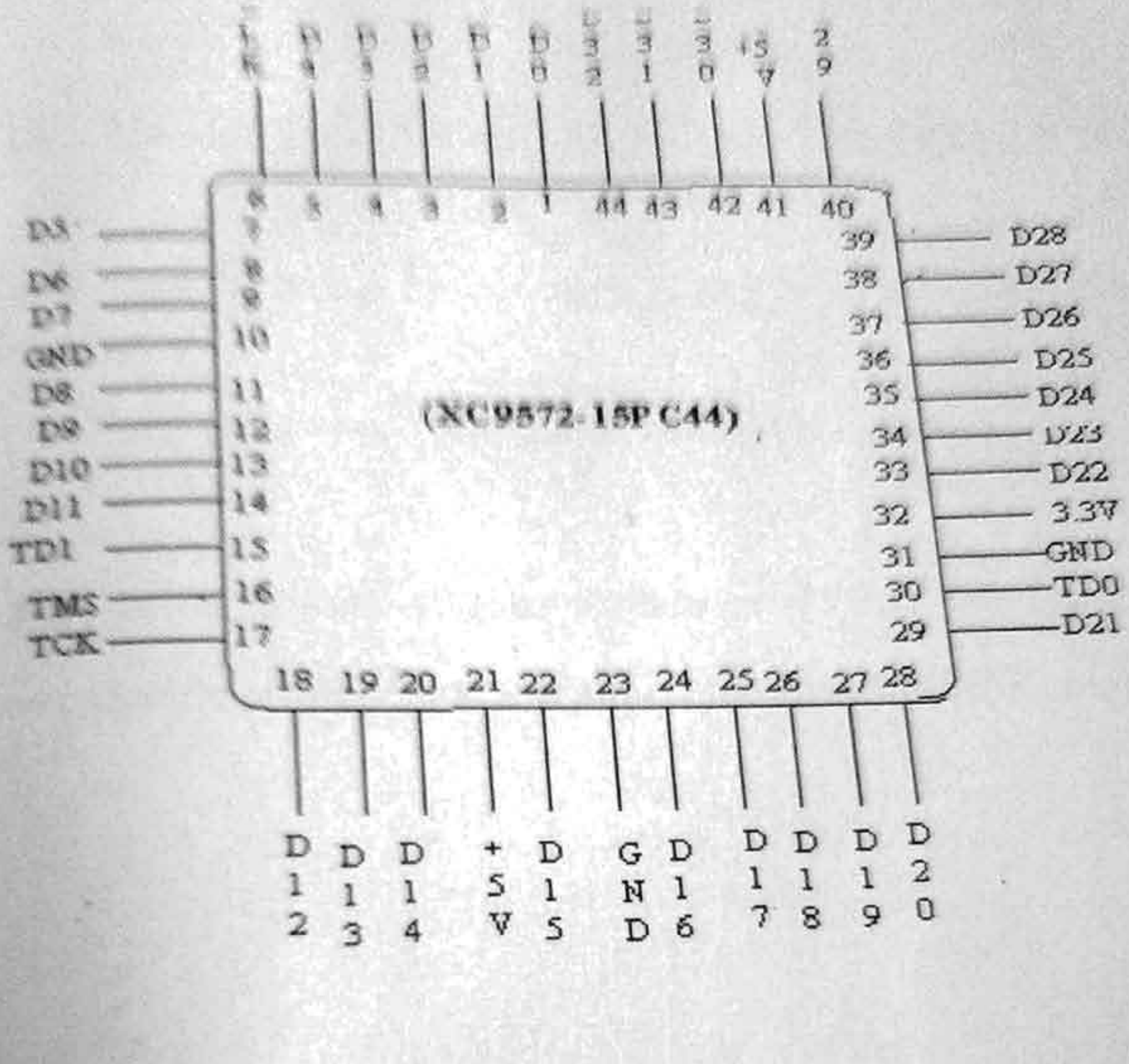

FIG NO.1

VCC = Dedicated Power Pin

GND = Dedicated Ground Pin

TDI = Test Data In, JTAG pin

TDO = Test Data Out, JTAG pin

TCK = Test Clock, JTAG pin

TMS = Test Mode Select, JTAG pin

***PROHIBITED* = User reserved pin**

***D0-D32*=input pins**

Xiljnx XC9500 CPLD family (XC9500XL & XC9500XV families)

XC9500 CPLD family provide advanced in system programming and test capabilites for high performance, general purpose integration. All device are in-system programmable for a minimum of 10,000 program erase cycle. IEEE 1149.1 JTAG boundary Scan support is also included on all family member. 36 576 register & 800 to over 12,800 usable gate

PBC & Product term Allocator

& Programmable AND array

* 18 independent macrocell each capable of implementing a combinational or registered function

STEPS TO USE XILINX AND PROGRAM THE CPLD DEVICE:-

Step 1: Start the Xilinx Project Navigator by using the desktop shortcut or by using

Start->programs-> Xilinx ISE->Project Navigator.

Step 2: In the project Navigator window go to FILE->New project

Give a specific project name and project location.Then click next.

FOR CPLD DEVICE SETTING:

Product Category:	All
Family:	xc9500CPLDs
Device:	xc9572
Package:	PC44
Speed:	-10

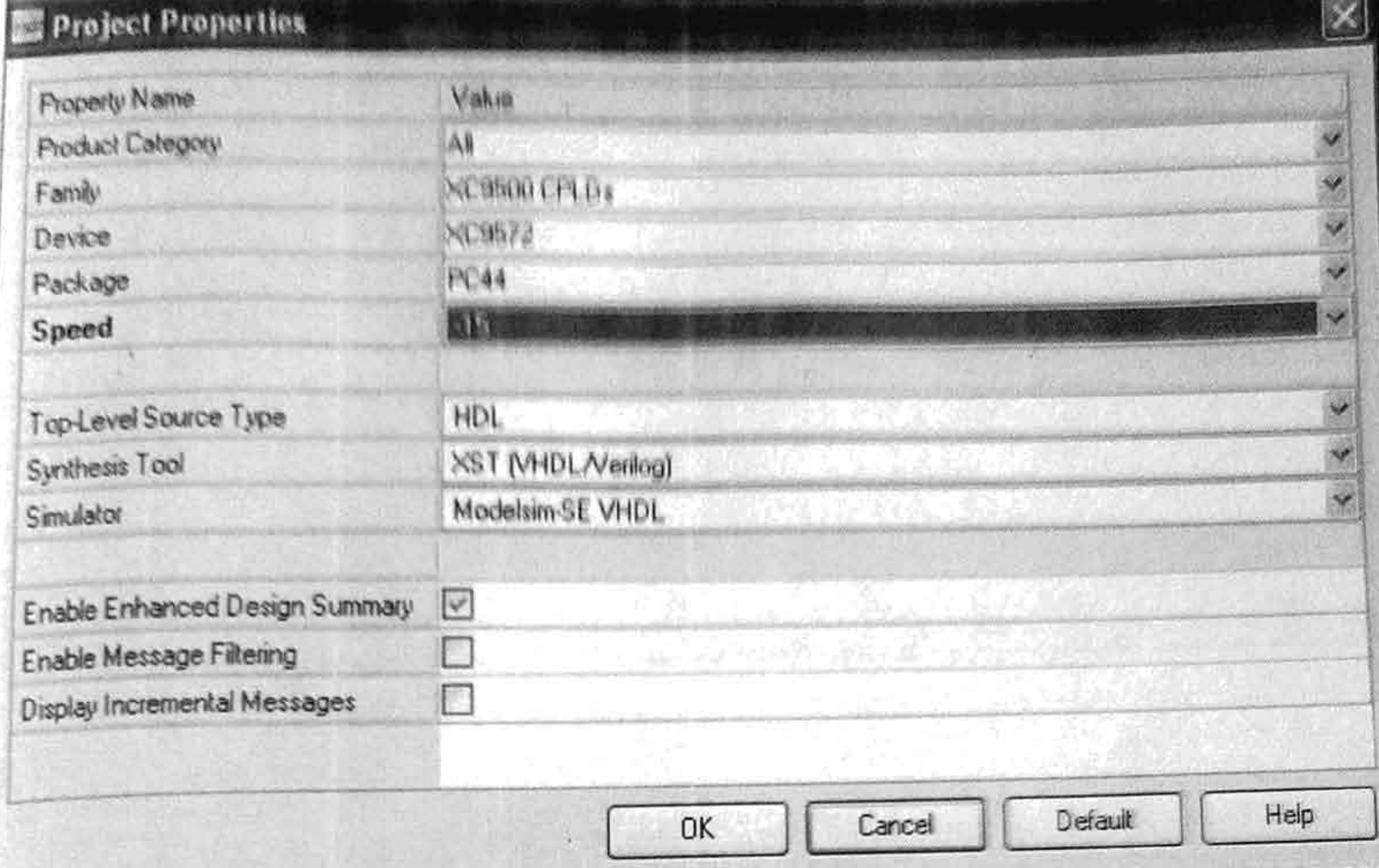

FIG NO.3

hen click next. In next window, click on new source. A new source
izard window will appear on screen.Here select VHDL module and
ive a particular file name and click next.

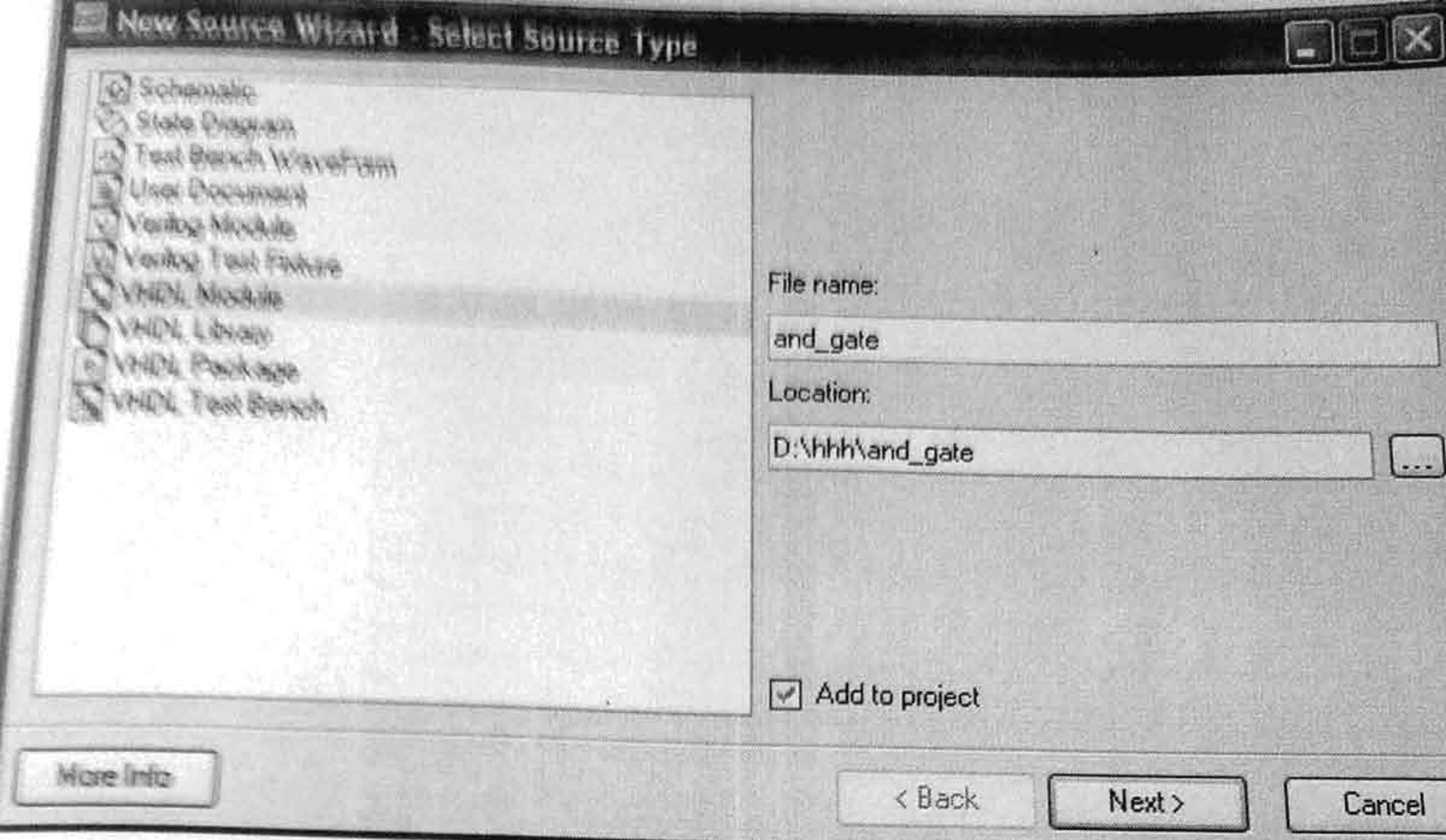

FIG NO.4

ep 4:- Define the ports in this window and click next.

w press finish.

n click next-->next-->finish.

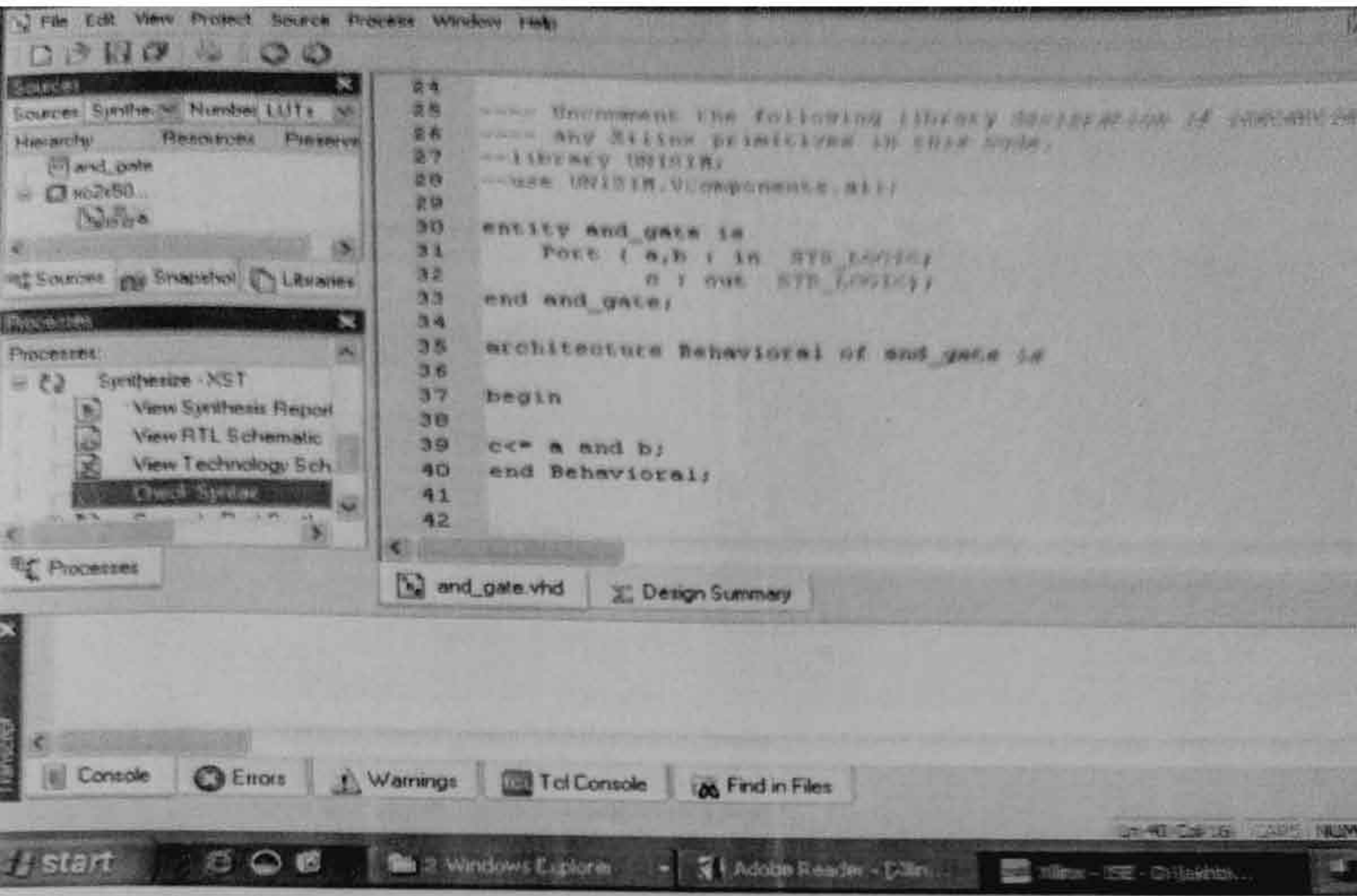

FIG NO.6

Step6: . Simulate the design using Modelsim.

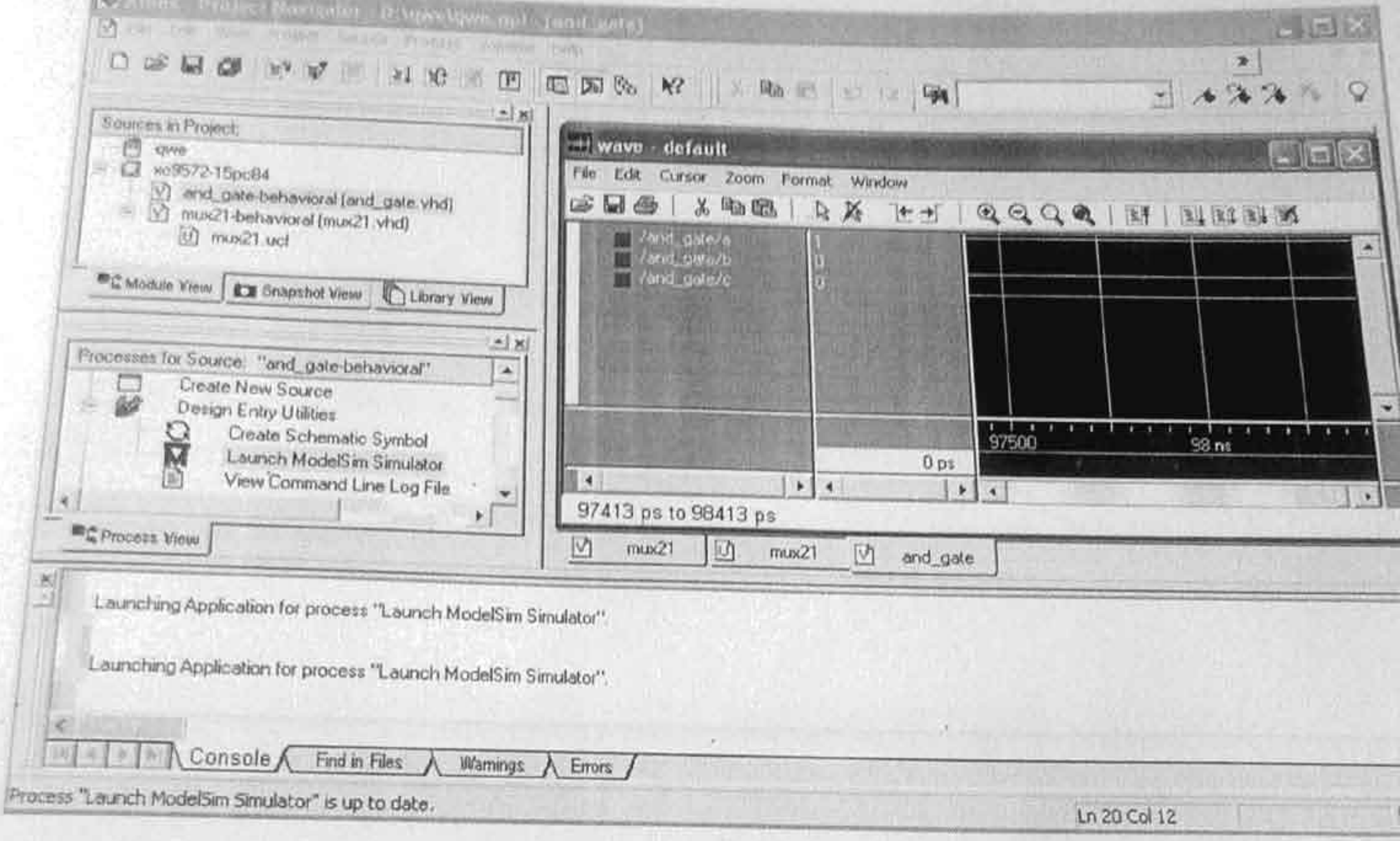

FIG NO.7

*entity->Finish->*Give inputs-> Click on simulate behavioral *model->*see the output.

Synthesis the design using XST.

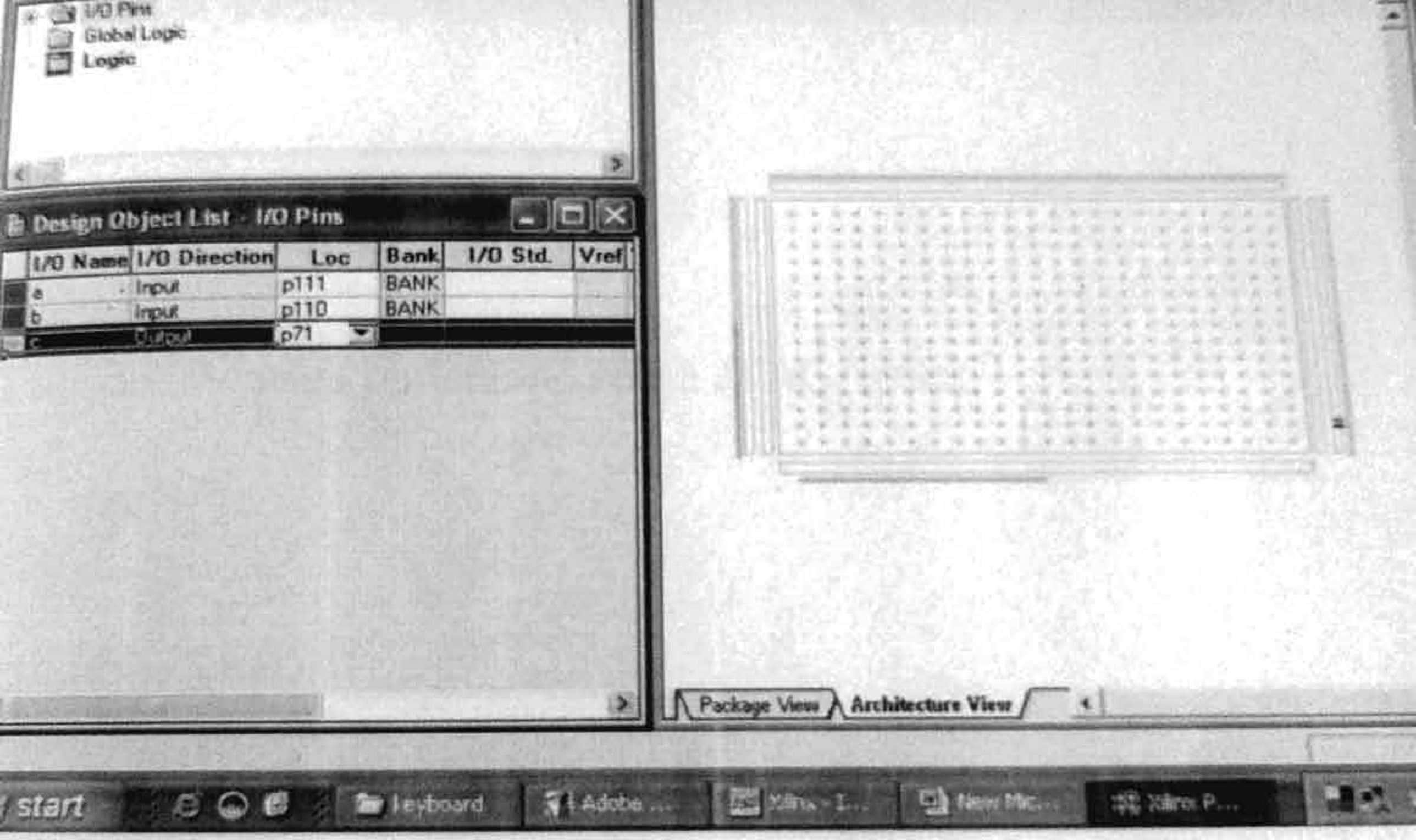

FIG NO.8 UCF window

hen go to startup option and select JTAG clock.

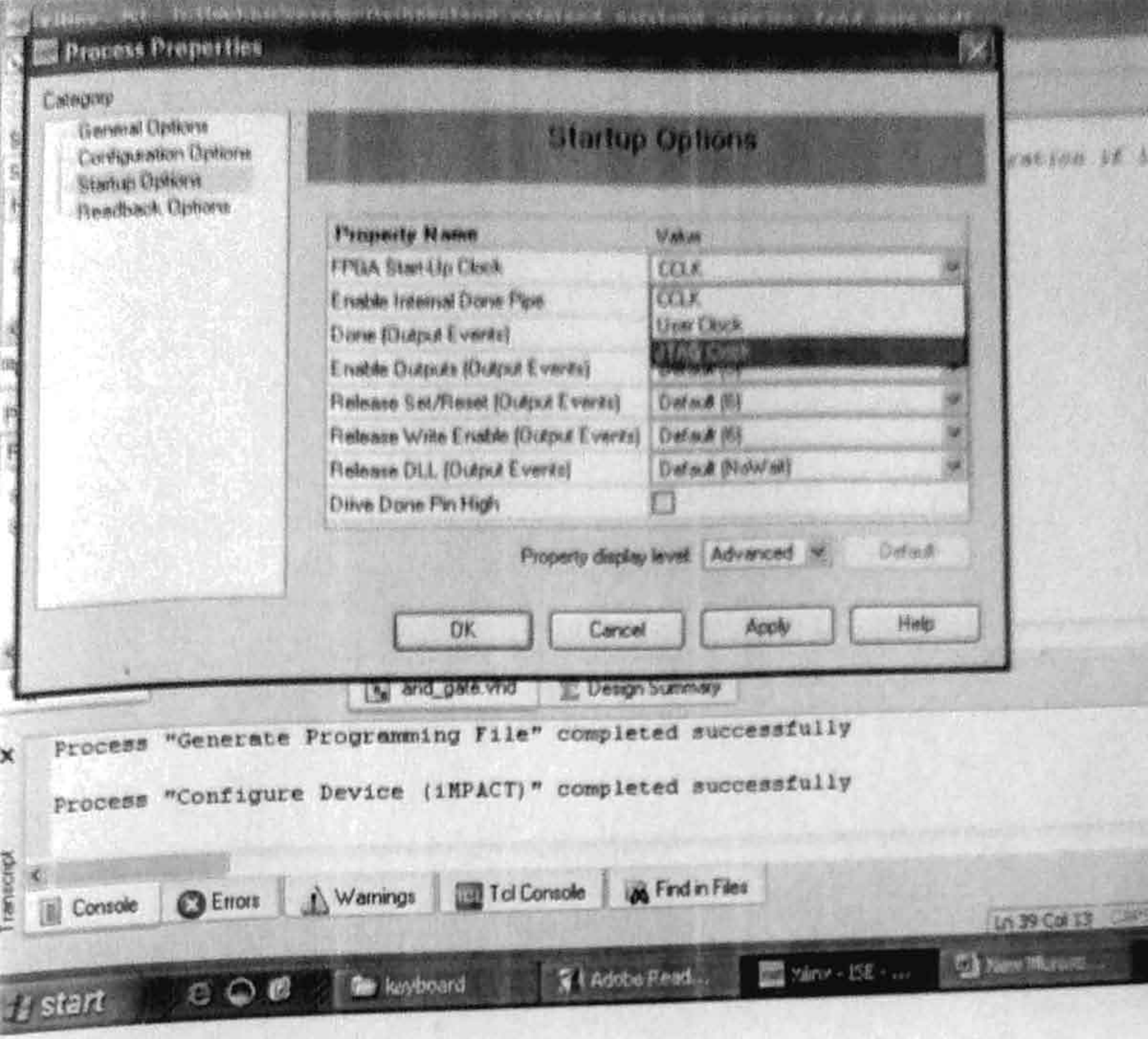

FIG NO.10

Step10: Run the Xilinx implementation Tools.

Once synthesis is complete, you can place and route yo